Data Converter Design in Simulink 5, Design Assessment

Design of an Audio Band ADC

Thomas Harley
s1810956

April 4, 2022

The University of Edinburgh
Sanderson Building
Robert Stevenson Road
The King's Buildings
Edinburgh
EH9 3FB

Contents

Chapter 1

Design Requirements

We are aiming to design an Audio Band Sigma Delta ADC. Before we can select the optimum modulator structure and specifications for our design, we must consider the system requirements in detail. These have been given in the assessment documentation [1]:

1. The following system specifications must hold true over the frequency range 20Hz - 20kHz.
2. A maximum stable input amplitude (MSA) of ± 0.85 for full scale input range ± 1.0.
3. Signal to quantisation noise ratio at MSA of at least 100dB.
4. Total harmonic distortion (THD) at input level 1dB below MSA should be less than -95dB.
5. No audio band limit cycles or tones that are greater than the quantisation noise power (no visible peaks above the noise floor).
6. Any valid modulator structure can be utilised including designs from the laboratories or custom designs.
7. Any sample rate can be used provided it is derived by dividing the master clock by a power of 2. The master clock is 24.576MHz (12.288MHz, 6.144MHz, 3.072MHz, 1.536MHz, etc.)

Additional requirements not expressly stated in the design brief, which have been reasonably assumed are:

8. The specifications are meant to be met for ideal conditions but the design should be resilient/ tolerant to typical non-idealities, for example an igain of 100, practical DAC element mismatch, coefficient mismatch.
9. When utilising a test frequency, it is best to choose one that allows the following relationship to hold:
$$f_t = \frac{C \times f_s}{N} \tag{1.1}$$
where C is an integer, f_s is the sampling frequency and N is the number of samples used in the FFT (default value is 8192). It is also better if f_t lies in the kHz range as it is easier to get good Power Spectral Density (PSD) estimates at higher frequencies. See table B.1 in the appendix for a full list of acceptable test frequencies for our final modulator.

Chapter 2

Justification of Modulator Structures/ Parameters

This section will consider various possible modulator structures and discuss their advantages and disadvantages. It combines the answers to questions 1 and 2 in the assessment documentation. MOD1 and MOD2 are briefly considered. MOD3 and MASH topologies are analysed in detail.

2.1 Considering MOD1 Structure

The first structure to consider is a first order modulator. Even though MOD1 has the advantage of being incredibly simple and cheap to implement, we can quickly discard it as a viable option for our design. Considering OSR value, the SQNR of MOD1 is fundamentally limited at realistic values. Theoretical SQNR is defined as:

$$SQNR = 6.02N + 1.76 + (20L + 10)\log_{10}(OSR) - 10\log_{10}\frac{\pi^{2L}}{2L+1} \tag{2.1}$$

where the number of bits in the quantiser $N = 1$, modulator order $L = 1$ and oversampling ratio is OSR [2]. To achieve an SQNR of 100dB in line with the assessment specification we require a minimum OSR of 1764. The nearest possible OSR value is 2048 (2^{11}). The power consumption from such a design would be highly impractical.

Additional problems with MOD1 include high susceptibility to tonal behaviour and DC limit cycles. The one advantage of MOD1 that we may try to utilise later is its inherent stability provided the input level is < 1.

2.2 Considering MOD2 Structure

The next structure to consider for our design is the second order modulator. Referring to equation 2.1, we can calculate the theoretically achievable SQNR for MOD2. A reasonable OSR value of 128 gives us a theoretical SQNR of $\simeq$ 106dB with multi-bit feedback (2-bit quantiser). Based on this OSR we can calculate our sampling frequency to be:

$$f_s = 2 \times OSR \times B \tag{2.2}$$

where B = 20kHz (signal band). We calculate the sampling rate to be 5.12MHz. The nearest allowable sampling rate is 6.144MHz. However, the actual maximum SQNR only reaches about 96.165dB in simulations. We can observe these results in figure A.1 in the appendix. The maxium stable amplitude (MSA) is -2 which corresponds to $10^{-\frac{2}{20}} = 0.794$. This falls short of the specification value which equals 0.85.

We may assume that by pushing OSR higher we can achieve our desired specifications with a MOD2. However increasing OSR greater than 128 is undesirable for a number of reasons [2]:

1. Higher power consumption to achieve short quantiser delays.

2. Higher required sampling frequency (f_s) since, according to equation 2.2, if we want to achieve a signal band of 20kHz, increasing OSR will require increasing f_s.

3. A sufficiently fast clock may not be available in the system, as we saw with MOD1 where f_s exceeded our master clock (24.576MHz). This means a modulator clock must be generated by adding a PLL, with additional costs and power demand.

Therefore, to achieve 100dB SQNR, using a higher order modulator such as MOD3 is better than employing MOD2 at a high OSR. The problem of high OSR is further explored in Chapter 6.

2.3 Considering MOD3 Structure

Now we consider third order modulators. If we implement MOD3 by simply adding a third non-delaying integrator (basic MOD3) we get an unstable output regardless of the DC or sine wave input. Therefore, we require a different topology.

2.3.1 Optimum Topology (CIFB, CIFF, CRFB, CRFF)

There are four main common architectures that we can utilise: Cascaded Integrators with Feedback (CIFB), Cascaded Integrators with Feedforward (CIFF), Cascaded Resonators with Feedback (CRFB) and Cascaded Resonators with Feedforward (CRFF). There are advantages and drawbacks of each topology. For our design, a CRFF was chosen. The feedforward architecture has the advantage of lower signal distortion and requires only one feedback DAC, which will increase simplicity of our design. This comes at the cost of higher power consumption than feedback but is a worthy tradeoff. The resonator structure was chosen over the integrator structure as it gives maximum SQNR improvement through better optimized placement of the poles/zeroes in the structure.

2.3.2 OSR Calculations

According to calculations using equation 2.1, a third order modulator with 2-bit quantiser and an OSR of 64 gives a theoretical SQNR of 118.85dB, which should meet our specifications. However, early testing indicated that with OSR = 64, the design could only just achieve the 100dB requirement with all conditions ideal. Therefore, if we want our solution to be robust enough to deal with various non-linearities and retain a 100dB peak SQNR then we need an OSR of 128 which has a theoretical SQNR equal to 139.93dB using a 2-bit quantiser.

We can also use Figures A.2 and A.3 [3] to get an esimate of the peak SQNR possible for 1 and 2-bit quantisers at various OSR values. Using equation 2.2 we calculate our optimum f_s for an OSR of 128 to be 5.12MHz with nearest valid f_s equal to 6.144MHz.

2.3.3 Multi-Bit Feedback/ Quantiser

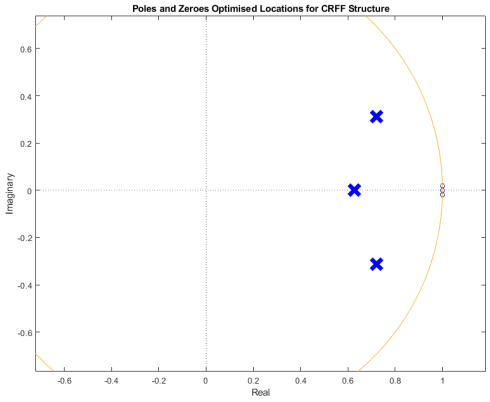
We must also choose an N-bit quantiser (2^N levels). As stated above a 2-bit quantiser should give a high enough SQNR to meet the design specification. One disadvantage of higher bit quantisers is that if our DAC feedback path is slighly imperfect (non-linear) our modulator performance will be significantly affected. This is why 3-bit or higher quantisers are not desirable. For the purpose of the design phase we will assume a perfect DAC, but as we will be testing how our design deals with imperfect conditions later (DAC element mismatch) it's important to bear this effect in mind.

A 2-bit quantiser comes with many benefits including reduced noise in the baseband which will result in a higher SQNR. Additionally, the quantiser gain is well defined for multi-bit designs. This is because there are more than two points to define the gain (see figure A.4 in the appendix). For a 2-bit quantiser there are 4 levels. This allows for a wider stable input range and will help us achieve our MSA of ± 0.85.

2.3.4 Optimum Coefficients (Schreier Toolbox Simulations)

Now we have decided on a third order, CRFF structure with OSR value 128 and a 2-bit quantiser we can use the "Schreier Delta-Sigma Toolbox" [4] to synthesise an optimised NTF. The MATLAB script used to produce these optimised coefficients is printed below. The `H_inf` input to the toolbox corresponds to the maximum out of band gain of the NTF. For 1-bit quantiser designs this can be estimated to be 1.5 based on Lee's criterion [5] but for multi-bit feedback designs the optimum value must be found using trial and error. In this case for an OSR of 128, the correct balance between maximum SQNR and stability ended up being 1.605. `umax` (the maximum input for our modulator) is also outputted by this script. For our CRFF, `umax` = ±0.9.

```
clear                % Clears all variables
init_vars3           % Initialises veriables

Order = 3            % Select modulator order
nLev = 4             % Number of levels of 2-bit quantiser
OSR = 128            % OSR value
H_inf = 1.605         % Maximum out of band gain of the NTF
form = 'CRFF'        % Topology

% Synthesize NTF, the "1" ensures we compute optimised zeros.
H = synthesizeNTF(Order, OSR, 1, H_inf)

% Finds optimised values for modulator coefficients
% a = feedback coefficients from quantiser to integrators
% g = resonator coefficients for finite NTF zeros
% b = feedforward coefficients from input to integrators
% c = forward path coefficients (between the integrators)
[a g b c] = realizeNTF(H,form)

% In order to implement "dynamic range scaling" must enable use of
% scaleABCD() function
% Must convert unscaled coefficients to ABCD format using this operation
ABCD = stuffABCD(a,g,b,c,form)

% Now we implement "dynamic range scaling" for our 2-bit (4-level) quantiser
% so that all signal outputs occupy range [-1, +1]
[ABCDscaled umax] = scaleABCD(ABCD, nLev,0,nLev-1)

% Generates model coefficients based on the scaled ABCD description
[a g b c] = mapABCD(ABCDscaled, form)
```



(a) Optimised Poles and Zeroes, OSR = 128

OSR	64	128
a_1	0.45893	0.57807
a_2	0.47615	0.98383
a_3	0.41978	1.0415
g_1	0.0059582	0.0018656
b_1	1.3794	1.0586
b_2	0	0
b_3	0	0
b_4	1	1
c_1	1.3794	1.0586
c_2	0.52776	0.30372
c_3	0.24262	0.19374

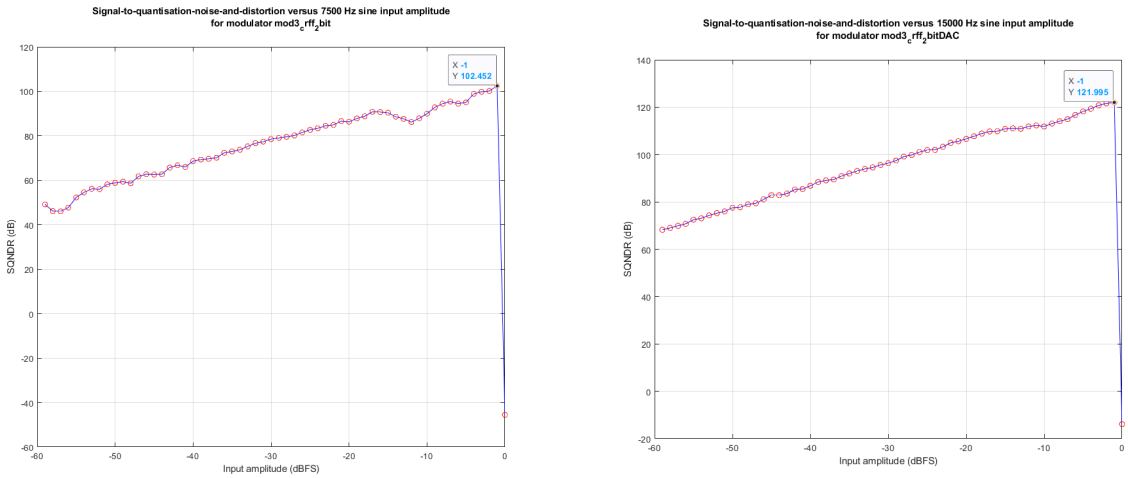
(b) Coefficients

Figure 2.1: Optimised Poles and Zeroes for CRFF Structure & Optimised Coefficients

This script produces optimised coefficients for our CRFF structure. Coefficients for OSR = 64 and 128 are shown in figure 2.1 above. A diagram showing the optimised locations of the poles and zeroes for the structure is also shown. Notice the zeroes do not all lie at DC.

Running some preliminary simulations, the results look promising. Examining figure 2.2, with $f_t = 15$kHz, we achieve a peak SQNR of 121.995dB which meets our specification. There is a large discrepancy between theoretical calculations (139.93dB) and actual performance. This is due to changing the location of the poles/ zeroes to achieve a stable MOD3. As a result, we suffer a reduction in SQNR. This is according to the Gerzon-Craven equal-areas theorem which establishes a trade off between SQNR and stability [2]. The peak SQNR is achieved at a MSA of -1dBFS which corresponds to a magnitude of $10^{\frac{-1}{20}} = 0.89125$. This meets our requirement of $> \pm 0.85$.

Also shown is the optimised simulation for OSR = 64 with $f_t = 7.5$kHz. We can observe why this design was not robust enough. Peak SQNR = $102.452dB$ which is just above specification at ideal conditions. It is unlikely this design could cope with component mismatches or other non-idealities hence the lower OSR is not viable. The higher OSR of 128 does come at the cost of higher power consumption.



(a) OSR = 64

(b) OSR = 128

Figure 2.2: Optimised MOD3 CRFF "sweep_sin_ampl_sqnr", 2-bit quantiser.

2.3.5 Dynamic Element Matching Scheme

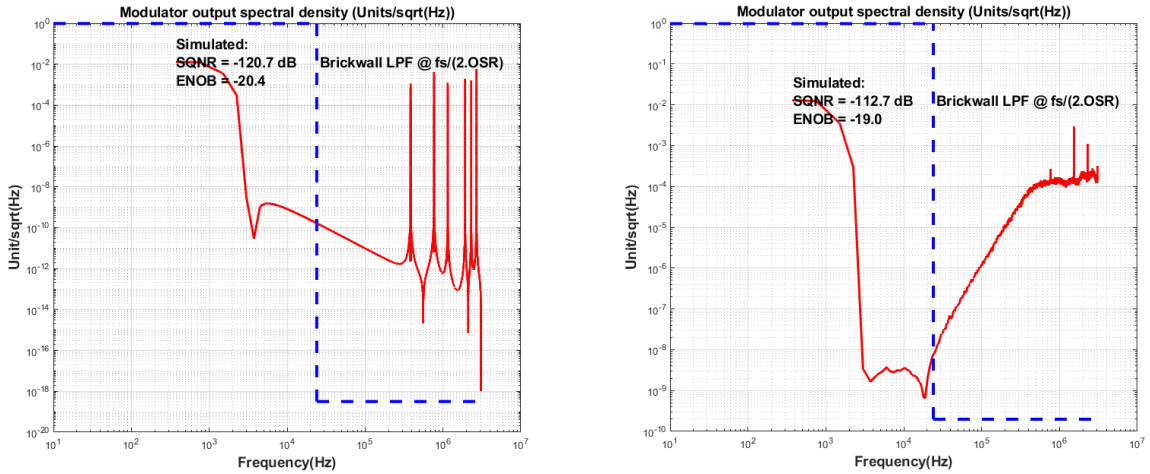
This design makes use of multi-bit feedback. Since this is an analogue modulator we require a DAC to convert the multi-bit quantiser output back to an analogue signal. For a multi-bit DAC to be perfectly linear we require perfectly matched components and therefore, real DACs are non-linear. We can use dynamic element matching (DEM) techniques to linearise real DACs. There are different DEM schemes that can be utilised in a design. Data weighted averaging (DWA), Individual level averaging (ILA), Butterfly scrambler and Random selection (RS). For this design DWA was chosen. DWA is the simplest to implement and results in better noise shaping and performance than an ILA based DEM [5]. More detail will be given in Chapter 4.

2.3.6 Dither Usage & Noise Shaping

We have illustrated that under ideal conditions this MOD3 CRFF structure can meet the design requirements. In terms of tonal performance, DC simulations show no visible spurious peaks rising above the noise floor in the audio band (baseband) at stable inputs. However, there are some

visible idle tones present outside the baseband, particularly for highly rational DC inputs. There is also very little noise shaping present. We will examine the performance with and without dither to ascertain its usefulness in our design. To add dither we issue the command below. A value of 0.05 was decided as adding too much will negatively impact MSA, and bring it below −1dBFS. We will test for a DC input of 0.5 (rational).

```
modctrl.dgain1 = 0.05          % Adds small amount of dither to our MOD3 DSM
```



(a) No Dither

(b) Dither = 0.05

Figure 2.3: DC Simulation of CRFF Structure, DC Input = 0.5

With the addition of dither, noise shaping is improved to $\simeq$ 80dB/decade. The visible tones outside the baseband have been removed. In addition, the sinewave sweep response has been further smoothed at lower amplitudes (< -35dBFS). It does come at a small cost to peak SQNR. However, our design comfortably lies above 100dB so this is not a concern.

2.3.7 Total Harmonic Distortion

As part of the system requirements we must ensure that total harmonic distortion at input level 1dB below the MSA is less than −95dB. We can calculate THD using the `MATLAB` function:

```
thd(Qout, Fs, n)          % THD function in MATLAB
```

where `Qout` is the time series output, `Fs` is the sampling frequency and `n` is the number of harmonics within the signal band given by:

$$n = floor(B/f_t) - 1 \tag{2.3}$$

where B is signal bandwidth. Since our f_s is 6.144MHz, B = 24kHz according to equation 2.2. f_t is given by equation 1.1 above. Setting the integer $C = 10$ we get $f_t = \frac{10\times 6144000}{8192} = 7.5$kHz. Subbing this into equation 2.3 above we get $n = 2$.

Now we run an AC simulation with an input level 1dB below MSA, which is −2dBFS ($10^{\frac{-2}{20}}$). Therefore `sinamp` is 0.79. The THD calculated from our `MATLAB` function with these inputs is equal to −155.10dB (see figure A.5 in the appendix). This is below the required level of −95dB.

2.3.8 Diagram of Structure

A diagram of the final MOD3 CRFF Optimised Structure is shown in Figure 2.4.

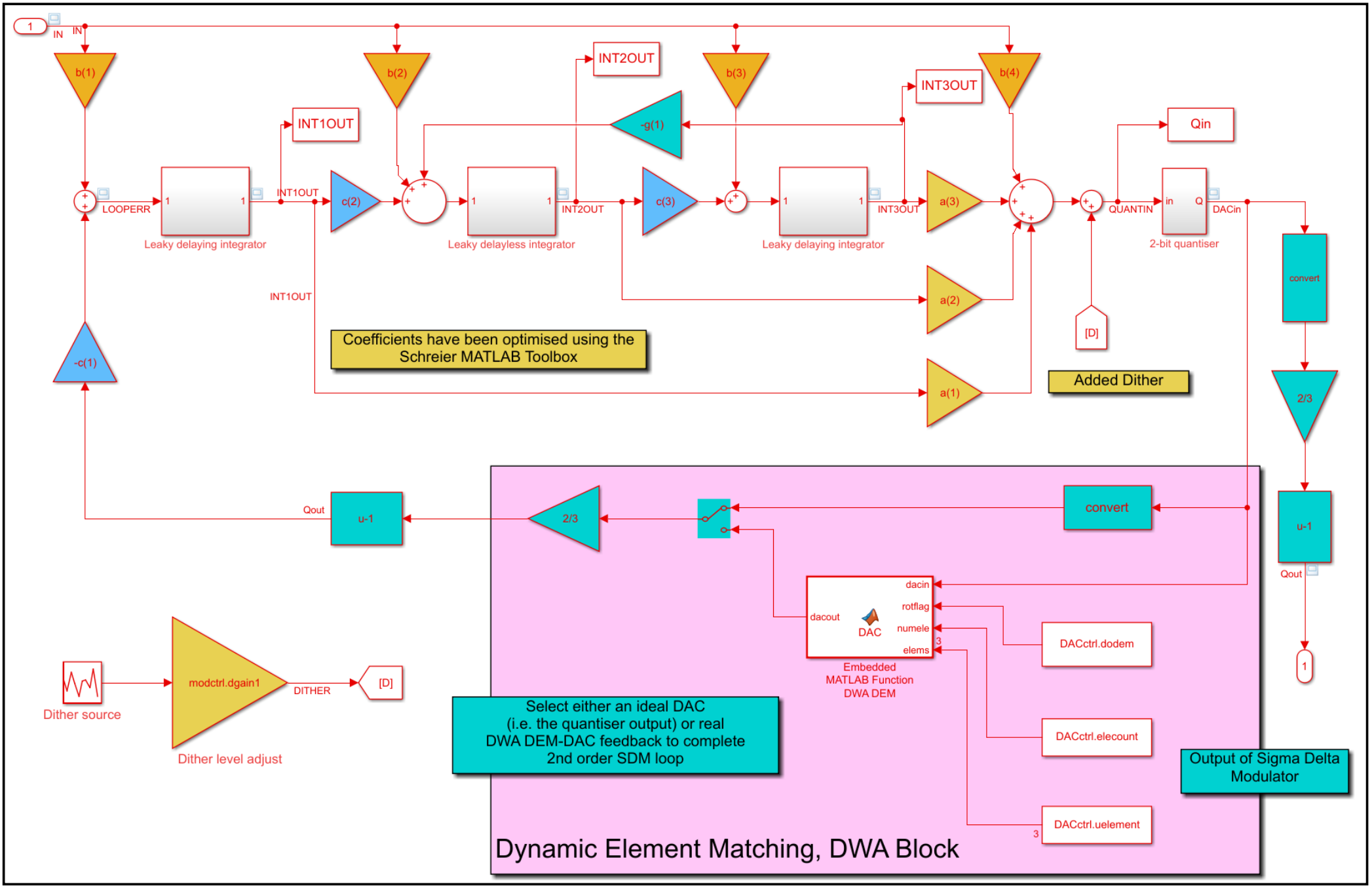


Figure 2.4: Schematic of Final MOD3 CRFF Design including DWA DEM-DAC

2.4 Considering MOD3 MASH Structure

The final structure to consider for our design is the MOD3 MASH structure. Unconditionally stable first/ second-order modulators are cascaded together to form a higher-order modulator.

2.4.1 Optimum Topology (1+1+1 MASH, 2+1 MASH)

There are two main topology options we can select. Firstly, the 1+1+1 which cascades together three MOD1 (first-order) loops to create a third order structure. Quantiser errors E1 and E2 from the first two stages are calculated by subtracting the quantisers' inputs from their outputs and are then fed into the next stage. These errors are cancelled when the digital outputs from all three modulators are recombined. This makes the 1+1+1 highly susceptible to non-idealities such as finite integrator gain and component mismatches. If the analogue implementation of the modulator does not match the digital arithmetic circuits used to recombine the modulators then the E1 and E2 error terms will not be perfectly cancelled leading to errors [2].

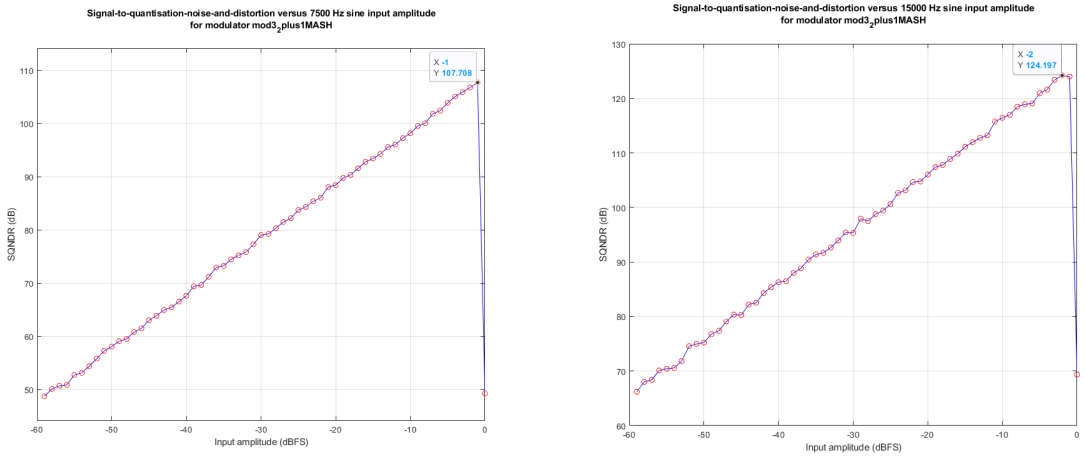
The 2+1 structure cascades a Steensgard-Silva MOD2 loop with a MOD1 loop to create a third order structure. This structure has several advantages. Firstly, the quantiser error of the first stage (E1) is available in the form '$-z^{-2}E1$' at the output of INT2. This removes the need for computation and reduces the chance of further error being introduced. Thus, the 2+1 is less susceptible to component mismatches and dead zones caused by finite gain (see figure A.6 in the appendix). The 2+1 MASH structure was also utilised to implement a 100dB SNR ADC in the audio CODECS of early Apple products. The 2+1 was chosen as the optimum topology.

2.4.2 OSR Calculations

All the OSR calculations for the 2+1 MASH are identical to the CRFF MOD3 as they are both third order modulators. Therefore, we will utilise an OSR value of 128 for a robust design, with a peak SQNR well above 100dB. This will allow the design to cope with reasonable non-idealities.

2.4.3 Multi-Bit Feedback/ Quantiser

In the case of the 2+1 MASH structure, we are making use of two different quantisers. A 2-bit quantiser for the Steensgard-Silva MOD2 stage and a 1-bit quantiser for the MOD1 stage. Since our error is based on the output of the 1-bit quantiser (E3) we sub N = 1 into equation 2.1. This gives us a theoretical SQNR of 112.83dB for OSR = 64 and 133.9dB for OSR = 128.



(a) OSR = 64

(b) OSR = 128

Figure 2.5: MOD3 2+1 MASH "sweep_sin_ampl_sqnr"

Simulating with these design values gives the preliminary results shown in figure 2.5 above. Test frequencies were 7.5kHz and 15kHz respectfully. These results indicate a slight improvement in peak SQNR over the CRFF structure. Again we see that with OSR = 64 our peak SQNR is quite close to our 100dB spec at ideal conditions (107.708dB), hence why this design is unfeasible. Looking at the results from OSR = 128, the peak SQNR is excellent at 124.197dB. However, our MSA is below spec at −2dbFS (0.79). In this regard the CRFF performs better. Its worth noting we can achieve an MSA of −1dBFS if we lower our testing frequency.

2.4.4 Dynamic Element Matching Scheme

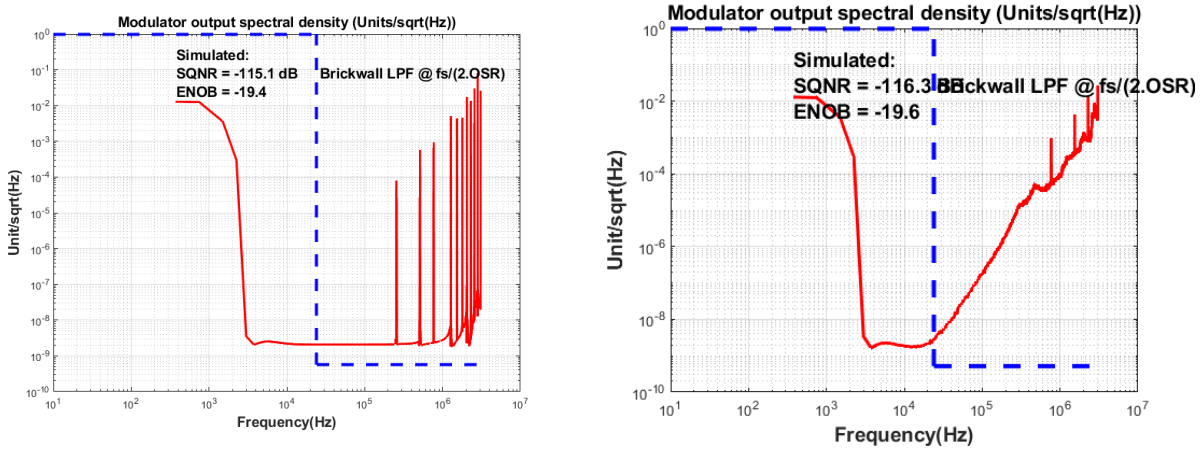
The DEM scheme employed for the 2+1 MASH is identical to the one employed for the CRFF structure. A DAC with a DWA algorithm is inserted into the feedback path of the Steensgard-Silva MOD2 structure. This structure uses a 2-bit quantiser and so requires a multi-bit DAC which will be non-linear with real components. Our DEM algorithm will help linearise our DAC.

2.4.5 Dither Usage & Noise Shaping

Using too much dither will further lower our MSA value so a very modest value of 0.05 (as was used for the CRFF) is a good place to start. For the MASH 2+1 we can choose whether to dither the MOD2 Steensgard-Silva (`modctrl.dgain1`) or the MOD1 (`modctrl.dgain2`). In this case we dither the MOD2. We will run a DC simulation as before with an input of 0.5. From this we can judge the effectiveness of dither. The structure does not seem particularly susceptible to DC "limit cycles". However, there are idle tones present at rational DC inputs as with the CRFF.

```
1  modctrl.dgain1 = 0.05          % Adds small amount of dither to our MOD3 DSM
```

By adding dither, we remove idle tones and produce noise shaping in the region of ≃ 80dB/decade.



(a) No Dither

(b) Dither = 0.05

Figure 2.6: DC Simulation of MASH 2+1 Structure, DC Input = 0.5

2.4.6 Total Harmonic Distortion

Total Harmonic Distortion for the MASH 2+1 structure is calculated the same way as the MOD3 CRFF. THD is equal to −146.17dB. This is below the required level of −95dB. Figure A.7 in the appendix shows the output from this simulation.

2.4.7 Diagram of Structure

A diagram of the final 2+1 MASH structure is shown in figure A.8

2.5 Comparison Table and Conclusions

We have now taken an incredibly detailed look at each modulator option for this design and examined their advantages and disadvantages. A summary of all the options considered, including their specifications and preliminary results from simulations are shown in table 2.1 below.

Specification/ Result	**MOD1**	**MOD2**	**MOD3 CRFF**		**MOD3 MASH 2+1**	
OSR	2048	128	64	128	64	128
Quantiser	1-Bit	2-Bit	2-Bit	2-Bit	1-Bit & 2-Bit	1-Bit & 2-Bit
DEM Scheme	-	-	DWA	DWA	DWA	DWA
Dither Value	-	-	-	0.05	-	0.05
Theoretical SQNR	101.94dB	106.26dB	118.85dB	139.93dB	112.83dB	133.9dB
Test Frequency (f_t)	-	15kHz	7.5kHz	15kHz	7.5kHz	15kHz
Peak SQNR (with Dither)	-	96.165dB	102.452dB	121.995dB	107.708dB	124.197dB
MSA (with Dither)	-	0.794	0.89	0.89	0.89	0.79
Noise Shaping (with Dither)	-	-	-	80dB/dec.	-	80dB/dec.
THD (with Dither)	-	-	-	-155.10dB	-	-146.17dB
`umax`	-	-	-	± 0.9	-	-

Table 2.1: Table Comparing all Modulator Options Considered in Chapter 1

From this table we discount MOD1 and MOD2 immediately as they fail to meet specification. MOD3 CRFF and MOD3 MASH 2+1 with OSR = 64 have peak SQNR values that are too close to 100dB. This means when we account for various non-idealities they will fall out of specification. Therefore we are left with two shortlisted options. MOD3 CRFF and MOD3 MASH 2+1 with OSR = 128. **The MOD3 with a CRFF structure was chosen as the final design** over the MASH for the following reasons:

1. The CRFF has a simpler design that requires fewer components such as quantisers. This will reduce component costs and area costs.
2. Better performance over a wide range of testing frequencies (f_t). The MASH modulators performance seems to deteriorate at higher frequencies.
3. Higher MSA that lies within specification (-1dBFS vs. -2dBFS).
4. The MASH Modulator suffers from additional non-ideal effects including the value of quantiser gain (we must be able to determine it accurately for the purposes of error cancellation) and signal path gain. This means the MASH will likely be more susceptible to analogue component mismatches when compared to the CRFF structure.
5. MASH modulator is more susceptible to finite DC gain when compared to CRFF (larger dead zones around DC input = 0).

While the CRFF does have some disadvantages, in general it is the superior option. The Schreier Toolbox has allowed us to create a perfectly optimised modulator for our requirements. In the following chapters we will examine the performance of this modulator in detail.

Chapter 3

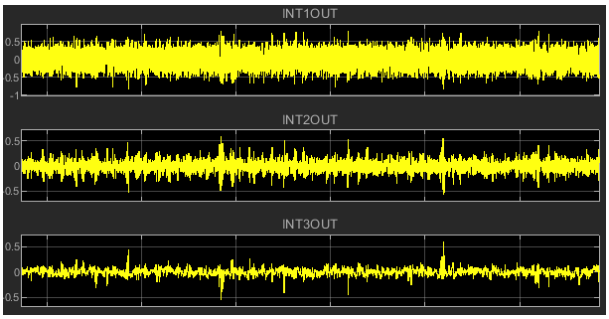
Simulations of Final Design assuming Ideal Characteristics

In this chapter we will look at how our CRFF modulator performs at "ideal" or "perfect" conditions. This section presents the answer to question 4 in the design assignment documentation. In particular, this chapter will demonstrate the modulator's stability and absence of limit cycle tones.

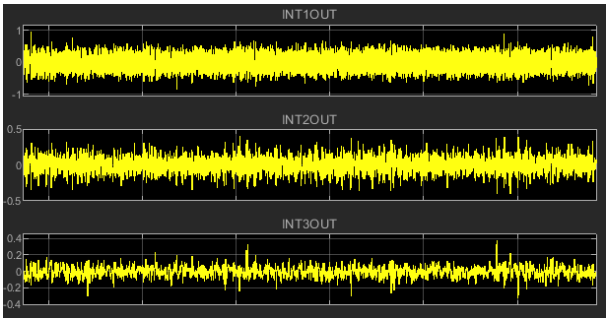
3.1 AC Simulations

3.1.1 Testing Frequency

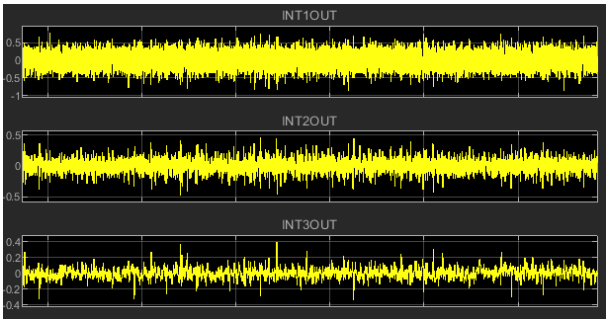
For a list of valid testing frequencies we can consult table B.1 in the appendix. We will test at four frequencies. $f_t = 7.5$kHz, 11.25kHz, 15kHz and 18.75kHz. We must demonstrate our modulator is stable over these frequencies. We run time domain simulations, setting `sinfreq` to our f_t values and examine our integrator outputs to ensure they are bounded. We will test at a sinamp of 0.9 as `umax` for this modulator was given as ± 0.9 in Chapter 2 (table 2.1).



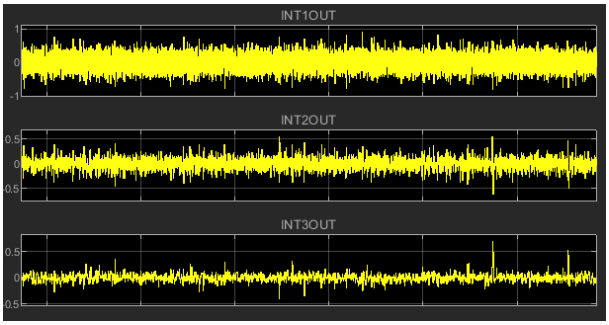
(a) $f_t = 7.5$kHz



(b) $f_t = 11.25$kHz



(c) $f_t = 15$kHz



(d) $f_t = 18.75$kHz

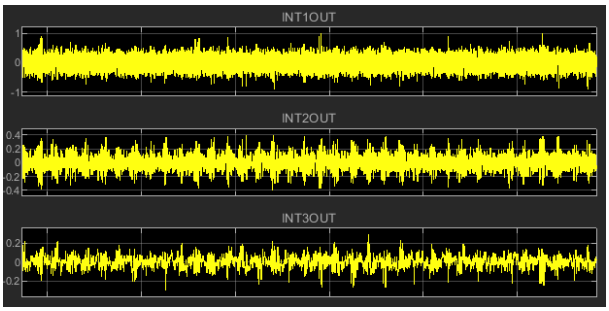
Figure 3.1: Time Domain Simulations, Integrator Outputs, sinamp = 0.9

From this we can see that our integrator outputs are bounded at all frequencies. Now we need to ensure that no limit cycles are present at these testing frequencies. We run a `Qout_SNDR` simulation at each frequency and check for tones in the passband. The figures generated show no

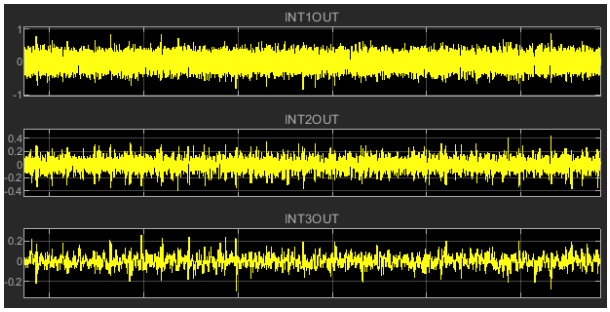
large tones. In addition, our integrator outputs in the time domain have no apparent repeatability which indicates there are no limit cycles.

3.1.2 Amplitude

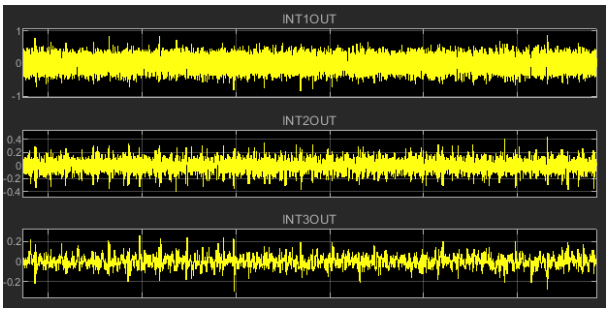
Now we will assess our modulator's stability over a range of amplitude (`sinamp`) values. We will keep our f_t = 15kHz for all these simulations. We will run simulations for `sinamp` = 0.25, 0.5, 0.75 and 1. Time domain outputs are shown below.



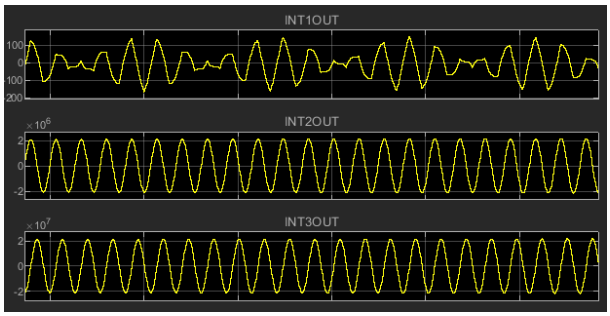
(a) `sinamp` = 0.25



(b) `sinamp` = 0.5



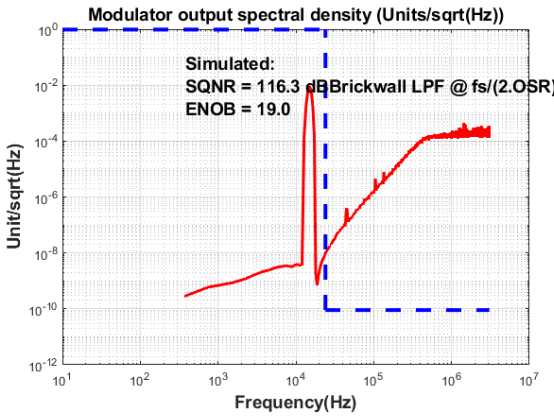
(c) `sinamp` = 0.75



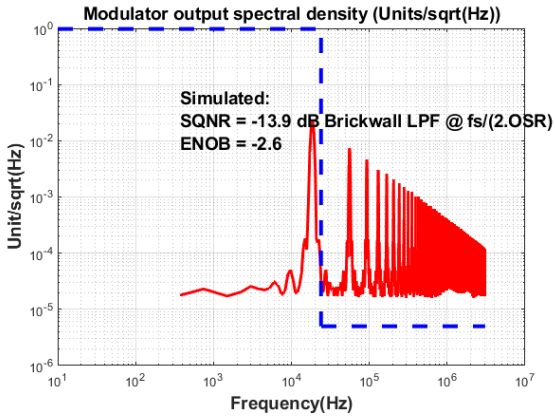
(d) `sinamp` = 1

Figure 3.2: Time Domain Simulations, Integrator Outputs, f_t = 15kHz

From figure 3.2 we can see that our modulator is stable for `sinamp` values 0.25, 0.5 and 0.75 as the integrator outputs are bounded. There is no repetition in the waveform which indicates no limit cycles are present. However, stability breaks down at `sinamp` = 1 which is above our maximum input amplitude quoted by `umax`. The integrator outputs are unbounded. Furthermore there is repetition of the waveform in the time domain. This would indicate the presence of limit cycles.



(a) `sinamp` = 0.5



(b) `sinamp` = 1

Figure 3.3: "Qout_SNDR", f_t = 15kHz

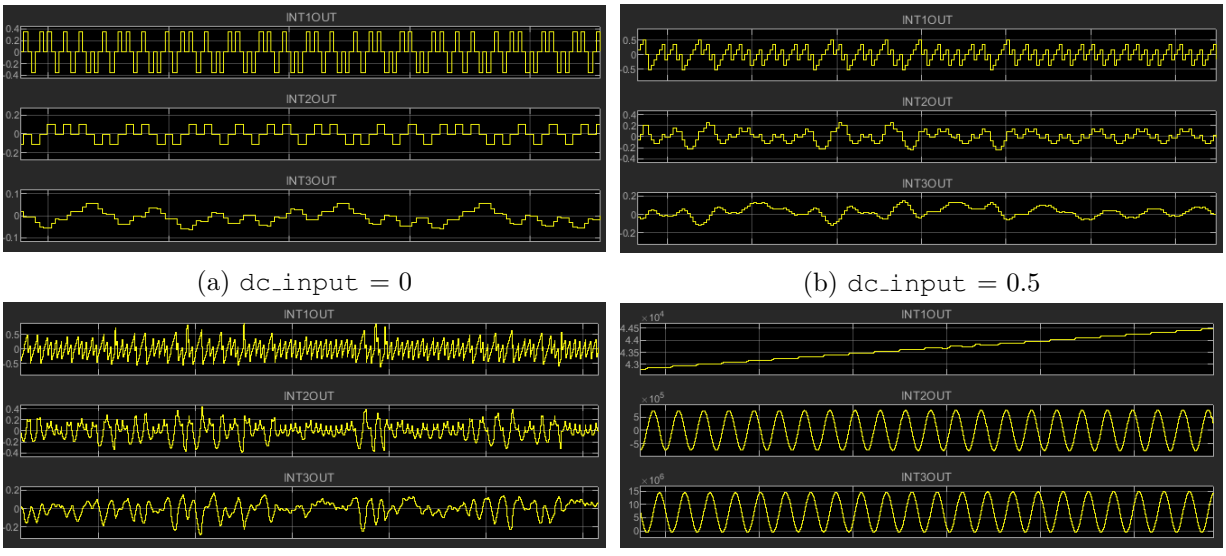
This is further supported by the `Qout_SNDR` simulations above which show many tones present in

the passband for `sinamp` = 1. For the other `sinamp` inputs, no tones are present. In Chapter 5 we will discuss the exact amplitude at which our modulator becomes unstable.

3.2 DC Simulations

3.2.1 DC Input

We will test the stability of our modulator at various DC inputs. Highly rational inputs are likely to have worse DC limit cycles and higher tonal presence. Our added dither of 0.05 should mitigate this as demonstrated in Chapter 2. We can use the `mean(Qout)` command to check if our DC output closely matches our DC input. We will test at `dc_input` = 0, 0.5 (highly rational), 0.4357 (less rational) and 0.98 (likely unstable). The time domain waveforms are shown below.



(a) `dc_input` = 0

(b) `dc_input` = 0.5

(c) `dc_input` = 0.4367

(d) `dc_input` = 0.98

Figure 3.4: Time Domain Simulations, Integrator Outputs, Dither = 0.05

We can see that all the dc input levels are stable apart from 0.98. For 0, 0.5 and 0.4367 the `mean(Qout)` shows the output is exactly reproducing the input. Comparing the highly rational input to the less rational input, we can see that there is less apparent cycling in the 0.4367 waveform which is to be expected. However, even for highly rational inputs, we can see from figure 2.3 in Chapter 2 that 0.5 has no obvious limit cycles present in the passband.

This slight apparent cycling could be a consequence of our very low value of dither (0.05) not breaking up all the tones present in the response fully. During the design phase a worthy trade off was made between having a higher dither and higher peak SQNR/ MSA.

The waveforms produced with DC input of 0.98 are highly unstable. The integrator outputs are unbounded. When we run `mean(Qout)` we get 0.7713 which shows our output is no longer reproducing the input. There is also clear cyclic patterns which will result in idle tones in the passband (figure A.9 in the appendix). Through extensive testing, the maximum stable `dc_input` level was found to be $\simeq 0.88$. This is almost equal to the `umax` value of ± 0.9.

3.2.2 Step Input

A step input block was added to the `sweep_testbench.mdl` structure in order to test step inputs. It was found that stepping from one input to another does not effect performance. Figure A.10 shows the time domain output of a simulation where `input_dc` has been stepped from 0.2 to 0.8.

Chapter 4

Simulations of Final Design including Non-Idealities

In this chapter we will examine the effects of typical non-idealities on our final modulator design. This section presents the answer to question 3 in the design assignment documentation.

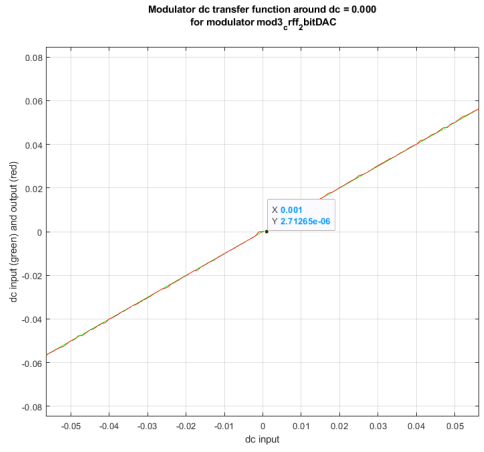
4.1 Finite DC Integrator Gain

We can set the finite gain for the three integrators in the MOD3 using the following command:

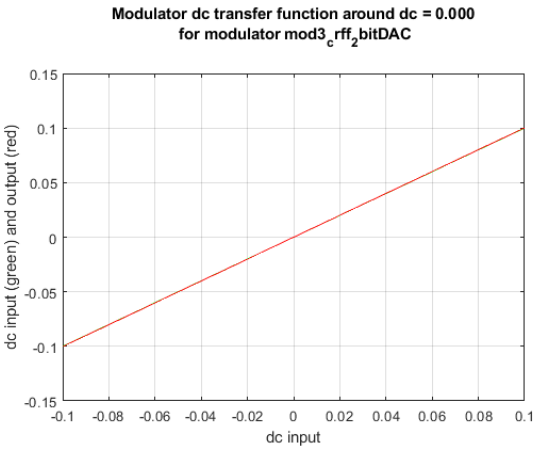
```
modctrl.igain1 = 10      % Can input igain2 and igain3 for other integrators
```

4.1.1 Examining Dead Zones

Generally at realistic integrator gain values, dead zones can appear around input_dc = 0. Dither can be used to remove small dead zones from our response. Let's examine dead zones present with and without dither by running a sweep for `igain = 10`.



(a) igain = 10 (all 3 integrators), No Dither



(b) igain = 10 (all 3 integrators), Dither = 0.05

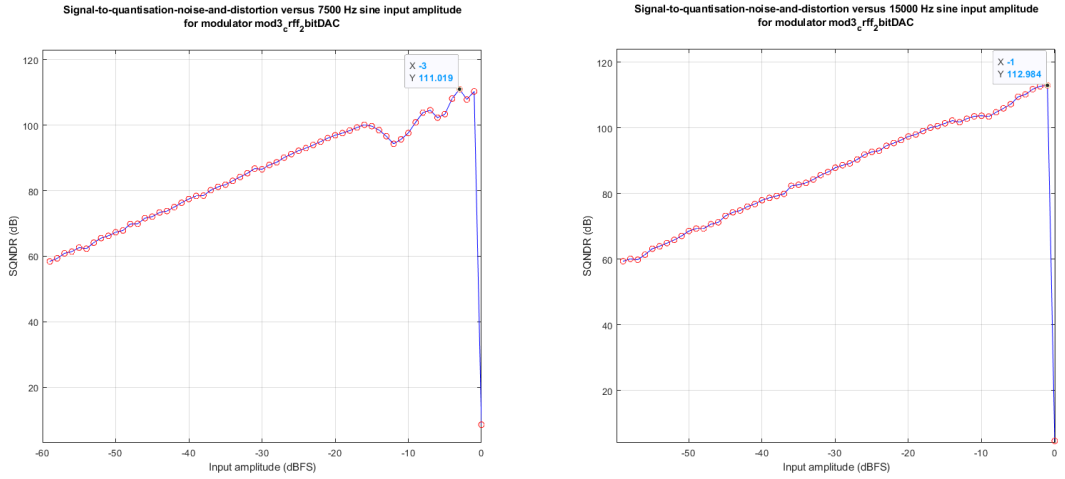
Figure 4.1: "sweep_dc_dc", Simulation from input_dc = −0.1 to 0.1

From the figure on the left, we can determine that with dither not present the width of dead zones for our MOD3 CRFF is proportional to $\simeq \frac{2}{A^3}$. For igain = 10, width is 0.002. This is an approximate relationship and will not always hold true as is the case for `igain = 5` where we would expect width of 0.016 and observe 0.012 (figure A.11 in the appendix).

Examining the figure on the right, dither has been applied with `modctrl.dgain1 = 0.05`. We see complete elimination of the dead zone. Therefore, dead zones will not have any real effect on our modulator since it will be trivial to achieve an `igain` above 10 in real implementation.

4.1.2 Examining Effect of Finite Gain on Peak SQNR & Noise Shaping

Lets examine a realistic `igain` of 100 and see if we can still achieve our required SQNR (100dB). We set the `igain` values as before. We will perform a `sweep_sin_ampl_sqnr` at two test frequencies.



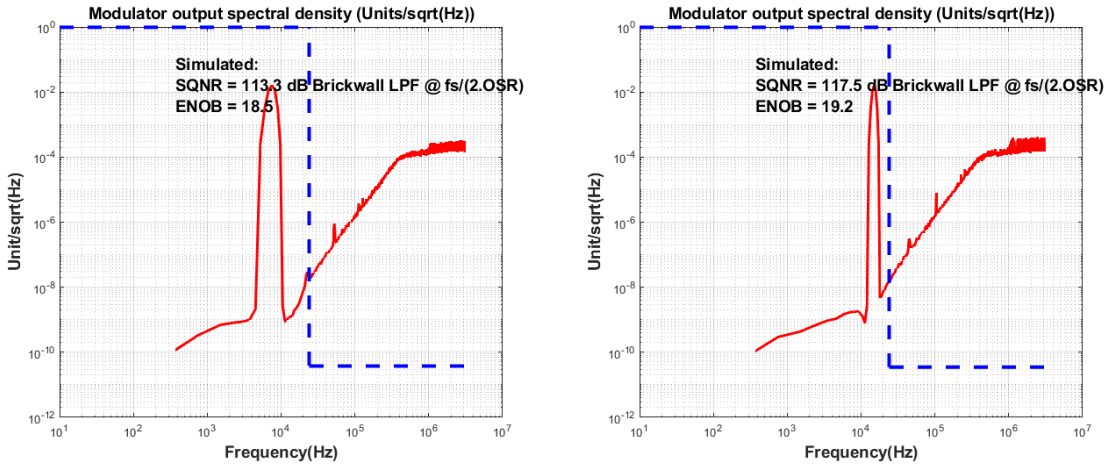
(a) $f_t = 7.5$kHz (b) $f_t = 15$kHz

Figure 4.2: "sweep_sin_ampl_sqnr", igain = 100, Dither = 0.05

At the lower test frequency there is a reduction in MSA to -3dBFS. We retain an MSA of -1dBFS at 15kHz. Our Peak SQNR drops by $\simeq$ 10dB to 111.019dB and 112.984dB respectfully. This is still well within specification. If we had employed a MASH 2+1, the drop would likely be more severe. The highly smooth plot at lower amplitudes shows that there are no dead zones present and that there are no tones present at low amplitudes (potentially removed by our dither of 0.05).

4.2 Coefficient Mismatch

When our CRFF is implemented in practice using analog components it is unlikely that our optimised coefficient values will be equal to their ideal values. It is generally safe to assume some level of non-ideality. Typical variation is about $\pm 1\%$ for a, b and c and up to $\pm 50\%$ for g. It was found that reducing the component values yielded the worst case performance. Coefficient values were set using the `MATLAB` code below.



(a) $f_t = 7.5$kHz (b) $f_t = 15$kHz

Figure 4.3: "Qout_SNDR", sinamp = 0.89, Coefficient Mismatch, Dither = 0.05

```
a = a*0.99; b = b*0.99; c = c*0.99; g = g*0.5;    % adjust coefficients
```

A `Qout_SNDR` simulation was run with sinamp equal to 0.89 and the results are shown in figure 4.3. We see a reduction in peak SQNR, of about 6dB in the case of $f_t = 7.5$kHz and 4.5dB in the case of $f_t = 15$kHz. This is to be expected. No real increase in tonal behaviour is observed.

4.3 Practical DAC Element Mismatch

As mentioned in Chapter 2, for multi-bit quantisers such as our design our feedback path will also be multi-bit. For analogue DSMs we require a DAC to convert the digital signal back to analogue. While ideal multi-bit DACs are linear as they use perfectly matched components, real multi-bit DACs will have some level of mismatch and therefore non-linearity. This will introduce an error and we must examine the effect of this on performance. For our simulations in Chapters 2 and 3 we used an ideal DAC. Now we switch to a real DAC by flicking the switch shown in figure 2.4.

4.3.1 Performance without Dynamic Element Matching

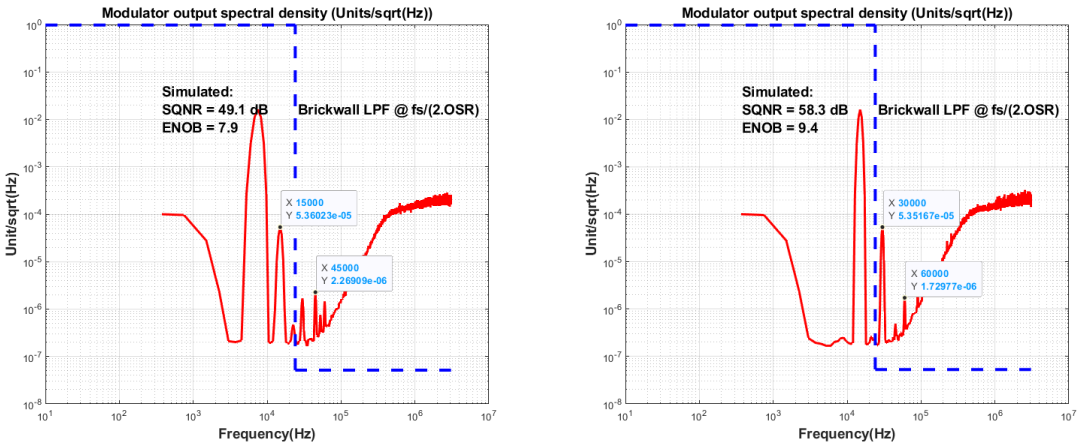
We use the `DACctrl.uelement` command in `MATLAB` to control the level of element mismatch. An ideal DAC would have values as follows.

```
DACctrl.uelement = [1, 1, 1]          % Control DAC Element Mismatch
```

Typical element mismatch for modern IC processes tends to be in the region of $\pm 0.025\%$ to $\pm 0.25\%$. We want to test the worst case scenario so will implement $\pm 1\%$. The following values were entered.

```
DACctrl.uelement = [1.01, 1, 0.99]          % Control DAC Element Mismatch
```

We keep the sum of the values = 3 so as not to introduce a small gain error. This way we can examine only the effects of non-linearity. We also ensure our dynamic element matching (DWA) is disabled by typing `DACctrl.dodem = 0`. We can then run `Qout_SNDR`.



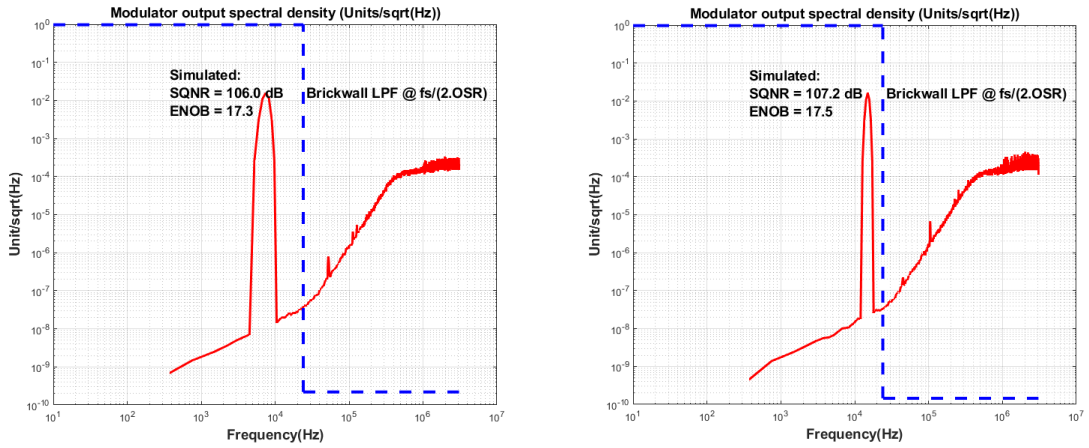
(a) $f_t = 7.5$kHz (b) $f_t = 15$kHz

Figure 4.4: "Qout_SNDR", sinamp = 0.89, DAC Element Mismatch, Dither = 0.05

This results in a complete collapse of SQNR which we would expect. Noise shaping has also suffered. DAC element mismatch also results in the generation of several harmonics of f_s at both testing frequencies. For $f_t = 7.5$kHz the largest harmonics are at 15kHz (present in the baseband) and 45kHz. For $f_t = 15$kHz the largest harmonics are 30kHz and 60kHz. This is not acceptable performance for our final modulator. We therefore use DEM techniques to counteract these effects.

4.3.2 Performance with Dynamic Element Matching

As discussed in Chapter 2, a Data Weighted Averaging DAC has been implemented in our modulator structure (see figure 2.4). DWA was chosen over Random selection (RS), Butterfly scrambler and Individual level averaging (ILA) due to its superior performance. DWA gives first order noise shaping and is also the easiest to implement. To enable DWA, we issue the `MATLAB` command: `DACctrl.dodem = 1`. Now we rerun the simulation and type `Qout_SNDR` to get the following plots.



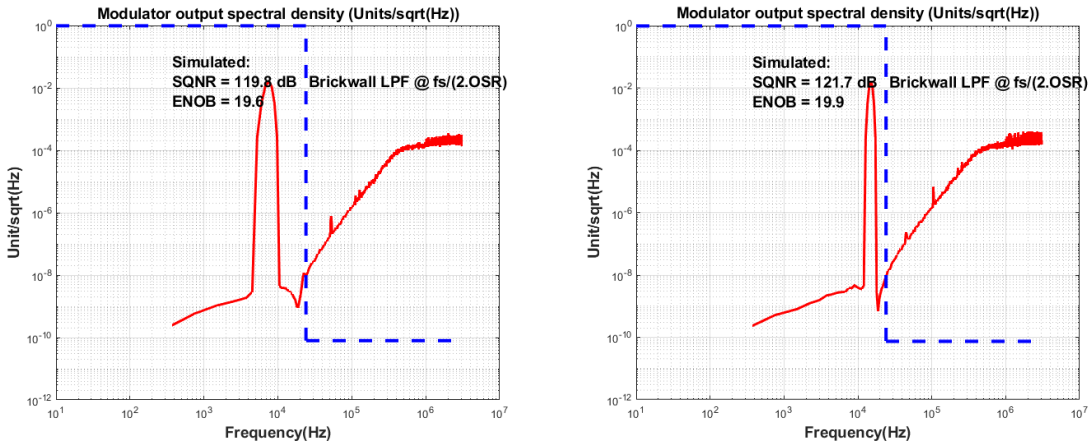
(a) $f_t = 7.5$kHz (b) $f_t = 15$kHz

Figure 4.5: "Qout_SNDR", sinamp = 0.89, DAC Element Mismatch with DWA, Dither = 0.05

We can see from figure 4.5 that original levels of noise shaping have been restored. The harmonic tones have also been removed by the data weighted averaging. However, SQNR is still lower than with an ideal DAC. There has been a reduction of over 10dB at both testing frequencies. The response is still within specification. One of the disadvantages of using DWA is it can cause limit cycle tones for DC inputs. However, a quick DC simulation reveals no tones have emerged.

4.4 Integrator Saturation

The integrator saturation variable limits the outputs of the integrators. In a practical circuit implementation, large outputs from the integrators would be clipped by the voltage rails. We set the `isat` values with the below `MATLAB` command which will limit each integrator's output to ± 1.



(a) $f_t = 7.5$kHz (b) $f_t = 15$kHz

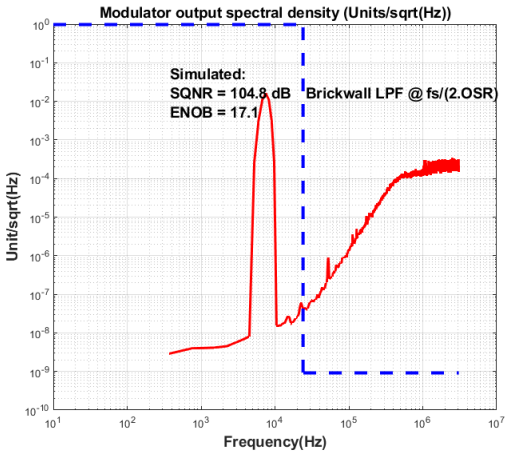
Figure 4.6: "Qout_SNDR", sinamp = 0.89, isat = 1, Dither = 0.05

```
modctrl.isat1 = 1       % Can input isat2 and isat3 for other integrators
```

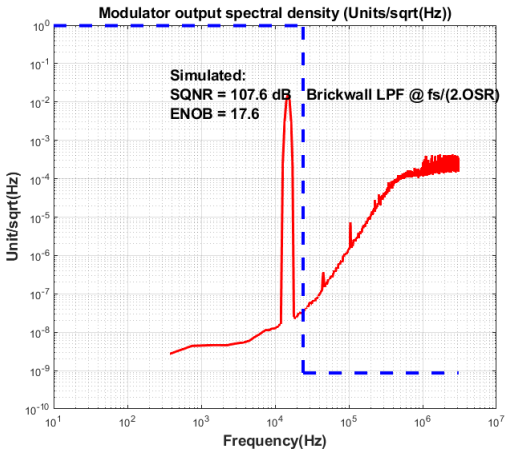
Our maximum amplitude (`umax`) value for this modulator is $\simeq 0.9$. Therefore we test to ensure that our integrators perform well up to this input level. Testing at `sinamp = 0.89` we produce the SQNR performance shown in figure 4.6 above. As we can see, the SQNR is not effected at all. This implies that all the integrators lie within the range of ± 1. This makes sense as when determining the coefficients for our MOD3 CRFF structure we employed dynamic range scaling to ensure that the integrator outputs would lie within the specified range. More detailed graphs of the integrator outputs as well as an in depth look at dynamic range scaling is given in Chapter 5.

4.5 Combining Non-Idealities (Worst Case Scenario)

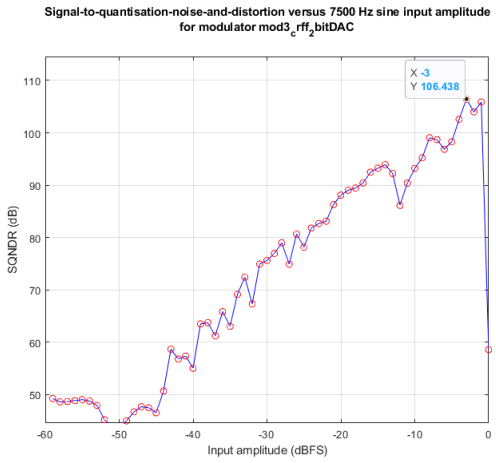
Finally we will consider a case where all these non-idealities are combined and demonstrate that under these conditions, our design can still meet the specifications given in the assignment briefing. Issuing all the lines of `MATLAB` code above, we set igain $= 100$, coefficient mismatch for a, b and c to -1% and g to -50%, DAC element mismatch $\pm 1\%$ and isat $= 1$. Then we run a `sweep_sin_ampl_sqnr` and `Qout_SNDR` command for both our testing frequencies.



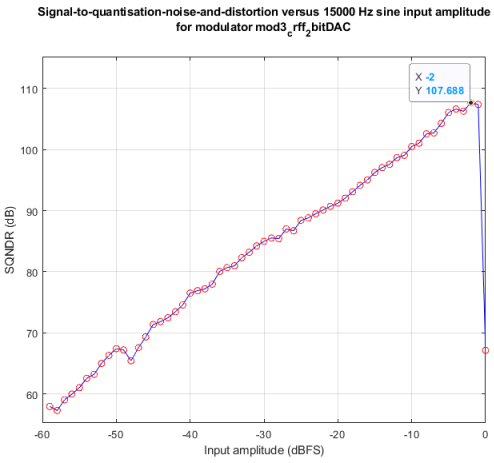
(a) "Qout_SNDR", $f_t = 7.5$kHz



(b) "Qout_SNDR", $f_t = 15$kHz



(c) "sweep_dc_dc", $f_t = 7.5$kHz



(d) "sweep_dc_dc", $f_t = 15$kHz

Figure 4.7: sinamp $= 0.89$ for (a) and (b), All non-idealities, Dither $= 0.05$

Overall these results are satisfactory and show our final modulator is highly robust. Combining all typical non-idealities, we still achieve a peak SQNR > 100dB. There is good noise shaping present in the passband and minimal tonal presence. However, our MSA has dropped slightly.

Chapter 5

Dynamic Range Scaling

In this chapter we will look at how dynamic range scaling can be added to our MOD3 CRFF design to improve performance. We will also determine the maximum stable input level. This section presents the answer to question 5 in the design assignment documentation.

Dynamic Range scaling is the process of scaling the integrator outputs of a delta sigma modulator so they lie within a certain specified range. Integrator outputs that are too large will be clipped in a real world application by power rails or other non-idealities. This will result in saturation and poor SQNR. Integrator outputs that are very small also have disadvantages. Integrator feedback capacitors become large which increases the area and cost of the integrated circuit. For these reasons we need to scale the integrators to an optimum level.

5.1 Implementation in MOD3 CRFF Structure

For the MOD3 CRFF, dynamic range scaling was performed during the design phase when the Schreier Toolbox was used to find the optimum coefficients. The command used is `scaleABCD()`. According to the Schreier Toolbox guide the arguments of this command are:

```
1 scaleABCD(ABCD, nLev, f=0, xlim, ymax)
```

Where ABCD are the scaled outputs, `nLev` is the number of quantisation levels, `f` is the normalised frequency of test sinusoid (typically 0), `xlim` is the limit on the integrators and `ymax` is the threshold for judging modulator stability (if the input exceeds this level, the modulator is deemed unstable).

5.1.1 Implementation for 1-bit Quantisers

Implementation for 1-bit quantisers (2 levels) is very simplistic. We can use the following command.

```
1 [ABCDscaled umax] = scaleABCD(ABCD, nLev)    % f = 0, xlim = 1, ymax is optional
```

The rest of the arguments are left as default. Since `xlim = 1` by default, this will scale our integrator outputs to lie within the ± 1 range. The two levels of the quantiser output will be -1 and 1. This command also outputs a `umax` variable which indicates the maximum possible input to the modulator before the integrator outputs exceed the specified limits and saturation occurs.

5.1.2 Implementation for N-bit Quantisers

The quantiser for our design is a 2-bit quantiser and thus has 4 levels. Implementing dynamic range scaling for multi-bit quantisers is slightly more complex. Most simulated quantisers have a fixed output range $[-1, 1]$ and then scale down the step size between quantiser levels depending on the value of `nLev`. An example is a step size of $\frac{2}{3}$ for a 4 level quantiser. However, the toolbox quantiser has a constant step size of 2. Its output range increases with the number of levels (`nLev`). Therefore, the modulator has a maximum input and output range of $\pm$`(nLev - 1)`. So for our 4 level quantiser, the maximum input becomes approximately $[-3, 3]$.

Now if we use the `scaleABCD()` command as before, the integrator outputs will scale to $[-1, 1]$. But, when we implement a normal quantiser with a fixed range $[-1, 1]$ and a variable step size, the integrator outputs will be scaled to $[-\frac{1}{3}, \frac{1}{3}]$ which is smaller than is desirable. Therefore the best option is to change the `xlim` value (scaling factor) in the `scaleABCD()` function to match the integrator range to the quantiser range. So `xlim = nLev - 1`.

```
[ABCDscaled umax] = scaleABCD(ABCD, nLev, 0, nLev-1)    % dynamic range scaling
```

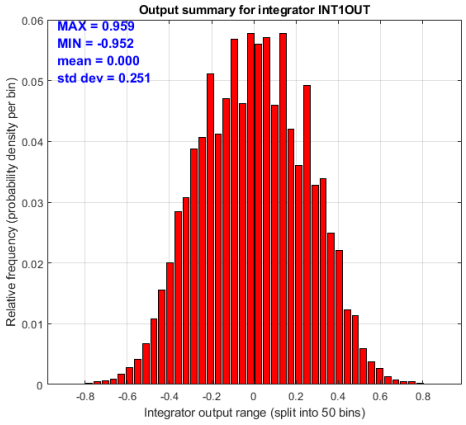
For our 4 level quantiser, when we replace the toolbox quantiser with a normal quantiser the integrator outputs will be scaled down to $[-1, 1]$. We need to divide the `umax` value given by 3.

5.2 Results of Dynamic Range Scaling

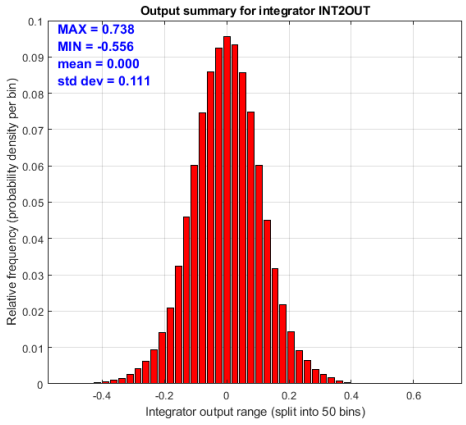
5.2.1 Integrator Outputs

We will now take a look at the result that dynamic range scaling had on the output of our DSM. We can observe the signal ranges for INT1, INT2 and INT3 of our modulator. We issue the following command in `MATLAB`. This command produces the following figures.

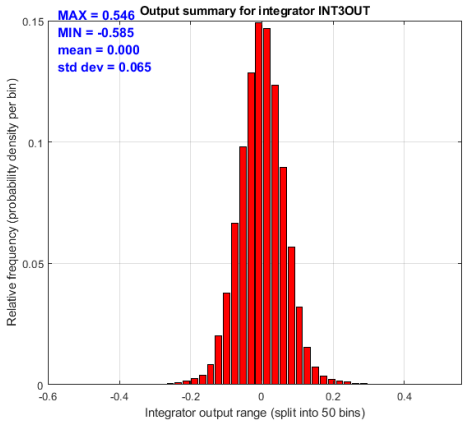
```
integ_stats(INT1OUT)        % Can input INT2OUT/ INT3OUT for other integrators.
```



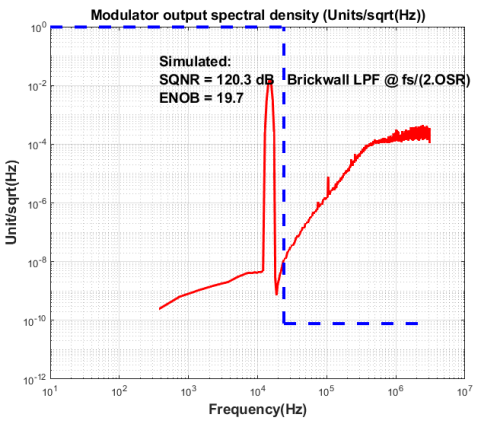
(a) INT1OUT



(b) INT2OUT



(c) INT3OUT



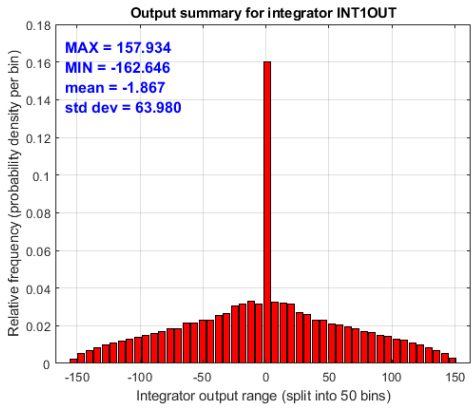
(d) "Qout_SNDR"

Figure 5.1: "integ_stats()", sinamp = 0.9, f_t = 15kHz Dither = 0.05

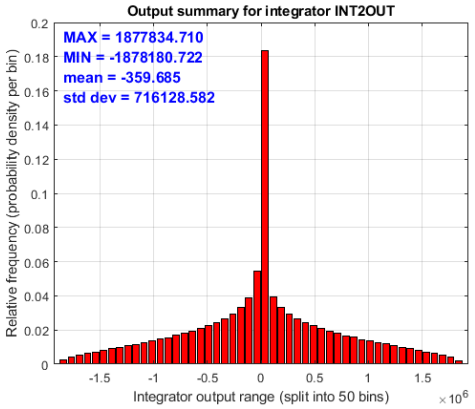
From the above figures we can see why setting `isat = 1` in Chapter 4 did not negatively effect the performance of our modulator. At input levels 0.9 and below, the integrators never exceed 1 and are well bounded. Also shown is a `Qout_SNDR` simulation which shows peak SQNR is achieved.

5.2.2 Maximum Stable Input Level

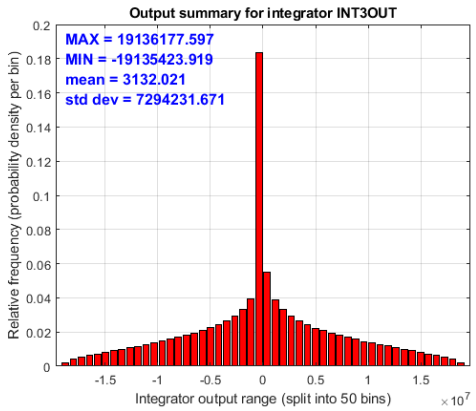
The `umax` output of the dynamic range scaling function was 2.7. Dividing this by 3 we get an estimated maximum input level of $\simeq 0.9$. If the input exceeds this level then the integrator values will no longer lie within the $[-1, 1]$ range. So 0.9 is our modulator's "maximum stable amplitude". However, stability does not completely break down until 0.95 is reached. Up until this point the integrator values remain somewhat bounded. The integrator responses for an input level of 0.95 are shown below. Also shown is the output of a `Qout_SNDR` simulation which shows complete collapse of SQNR with unstable integrator outputs. These figures show that the absolute maximum amplitude for this DSM is < 0.95.



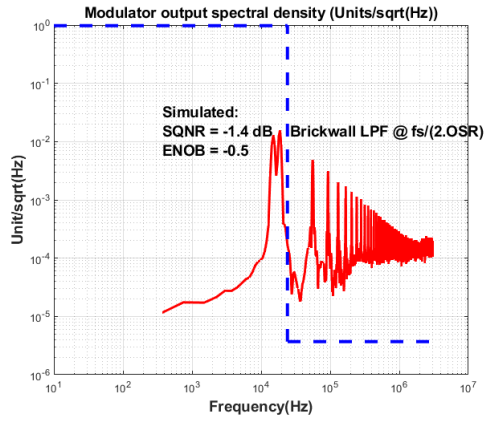
(a) INT1OUT



(b) INT2OUT



(c) INT3OUT



(d) "Qout_SNDR"

Figure 5.2: "integ_stats()", sinamp = 0.95, f_t = 15kHz, Dither = 0.05

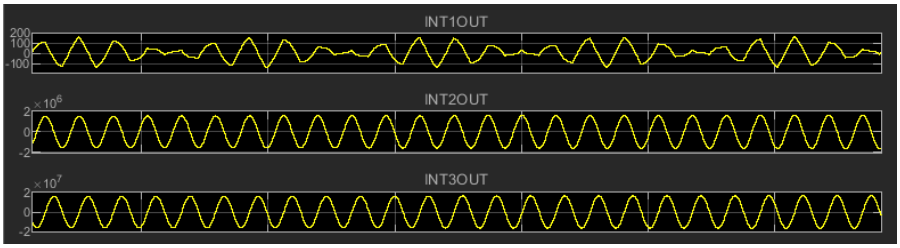


Figure 5.3: Time Domain Waveforms of Unstable Integrator Outputs, sinamp = 0.95

Chapter 6

Discussion

From the above chapters, it is clear our final design for an audio band ADC performs as required. This chapter contains some final discussion points on the merits and drawbacks of our design. This section presents the answer to the second part of question 3.

6.1 Power/ Speed Considerations

Firstly, considering power consumption. It is related to both OSR value and modulator order. For very high values of OSR, power consumption will be excessively high in order to achieve quick settling of the integrators. This is one of the primary reasons why utilising a MOD2 with a very high OSR to achieve an SQNR of $\simeq 100$ is less effective than a higher modulator order, with a lower OSR. Our final MOD3 design has an OSR value of 128. A MOD4 structure with an OSR of 64 would consume less power (modulator order effects power less than OSR) and may have similar performance. However, we choose not to employ such a structure due to area cost considerations.

Secondly, considering speed requirements. This relates primarily to the required slew rate of our input op-amps. At higher levels of OSR we require higher slew rate, particularly if high amplitude signals are being input to the integrators. With an OSR of 128 our slew rate will be quite high. However, the number of bits in the quantiser also effects our speed requirements. Our design has a multi-bit quantiser (2-bit). This will reduce the required slew rate of the op-amp at the input of the DSM's loop filter. This is because the input to the DAC changes less from sample to sample. Our feedforward architecture (CRFF) will also reduce slew rate requirements.

6.2 Area Cost Considerations

When considering the final design we must also look at how much area on an IC the DSM would take up. One consideration is number of integrator stages. Our final MOD3 CRFF structure has three integrators. This is one of the advantages of choosing a MOD3 at a higher OSR over a MOD4 at a lower OSR. The reduced number of integrator stages will reduce area cost. However, this may not be too important depending on the size of process technology being used to fabricate the DSM. Our final design also makes use of a Data Weighted Averaging DEM scheme to linearise the multi-bit feedback path. This will increase area cost.

Another metric that effects area cost is the range of our integrator outputs. If our integrator outputs are too low $[-\frac{1}{3}, \frac{1}{3}]$ instead of $[-1, 1]$, as mentioned in Chapter 5, then the feedback capacitors for the integrators will have to be very large, taking up more chip area. However, since we have implemented dynamic range scaling to optimise our integrator outputs to the highest level without saturation occurring, this is unlikely to be a problem. Finally, opting for a MOD3 structure with feedforward architecture (CRFF) over one with feedback architecture (CRFB) keeps area costs lower since there is only one feedback path. Therefore, only one DAC and dynamic element matching scheme is required on the integrated circuit. The CRFF will also have a lower cost than MASH structures as less components (such as quantisers) are required to implement the architecture.

Chapter 7

Evaluation of a Delta Sigma ADC Found in Literature

In this chapter we will examine a Delta-Sigma ADC from literature with an application other than audio. This section presents the answer to question 7. The title of the paper is: "Analysis and System-Level Design of a High Resolution Incremental ΣΔ ADC for Biomedical Applications" [6].

7.1 Description & Diagram of Structure

7.1.1 System Requirements

A summary table of the design specifications given by the authors is shown below (table 7.1) [6].

Specification	Value
Signal Bandwidth (f_b)	3.5kHz
Number of Channels (N_{ch})	20
SNR	98dB
Maximum Stable Amplitude (MSA)	−6.02dBFS
Sampling Frequency (f_s)	20.48MHz
Required Bit Resolution (n_{bit})	$6-16$ bits

Table 7.1: System Requirements of Sigma Delta ADC from Literature

7.1.2 Modulator Structure/ Parameters

A fourth order modulator (MOD4) with a 1-bit quantiser was chosen by the designers. A feedforward summation structure (CIFF) has been utilised which allows better optimisation of poles and zeros. As mentioned in the specifications, high bit resolution is very important for this modulator. The resolution of the modulator is loosely given by the following equation (derived in [6]):

$$n_{bit} = \log_2(V_{inmax}\frac{N(N-1)(N-2)(N-3)}{4!}\frac{c_3c_2c_1b}{V_{ref}}) \tag{7.1}$$

FeedForward Coefficients		Integrator Coefficients	
a_1	1	c_1	0.52
a_2	1.54	c_2	0.31
a_3	1.12	c_3	0.19
a_4	0.76	b	0.52
a_5	0.39	-	-

Table 7.2: Optimised Coefficients for MOD4 Structure from Literature

The authors targeted a resolution of 17 bits, in order to guarantee a resolution of 16 bits once non-linearities were taken into account. They used equation 7.1 in combination with the MATLAB

Schreier Toolbox to determine the optimised coefficients for the modulator (table 7.2) and the OSR value (referred to as N in [6]) which equals 127.

7.1.3 Diagram of Structure

A Simulink block diagram was created to model the modulator as described in the paper. A diagram of this is shown in figure 7.1. The modulator described in the paper also has a digital filter which was not implemented in our Simulink model.

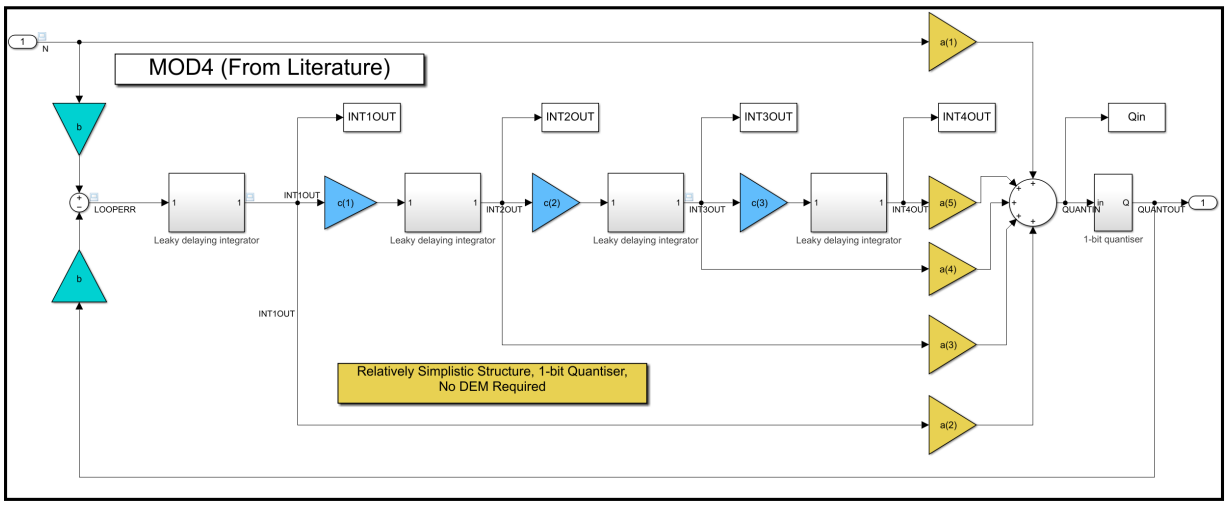
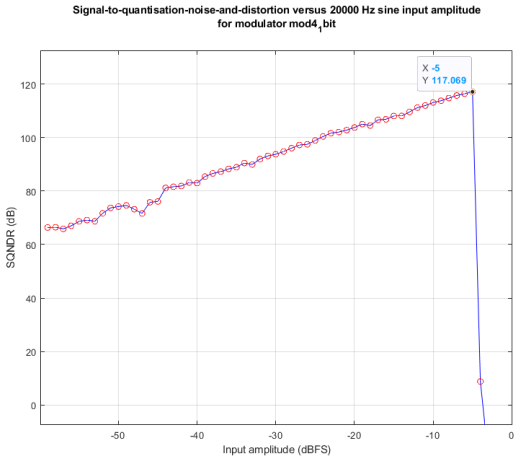


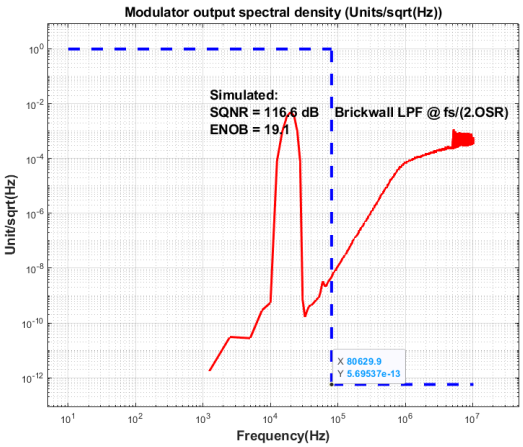
Figure 7.1: Fourth Order CIFF Sigma Delta ADC for Biomedical Applications

7.2 Simulink Simulation of Sinewave Amplitude Sweep Test

Simulink simulations were used in this paper to determine the performance of the modulator. Using the simulink block diagram shown above we will run `sweep_sin_ampl_sqnr` and `Qout_SNDR` simulations and compare these to the results in [6]. We need to determine our f_s value. Setting it to the value given in table 7.1 (20.48MHz) gives us a bandwidth of 80.6kHz according to equation 2.2. We will set `sinfreq` (f_t) to 20kHz and our `sinamp` to -6.02dBFS or 0.5. These were the testing conditions used in [6]. We produce the figures shown below in figure 7.2.



(a) "sweep_sin_ampl_sqnr"



(b) "Qout_SNDR", sinamp = 0.5

Figure 7.2: Simulation Results for MOD4 from Literature, $f_t = 20$kHz

Our simulated sweep is very smooth at lower amplitudes which implies no tones are present and this is supported by our `Qout_SNDR` simulation which shows good noise shaping of $\simeq$ 80dB and no visible tones. We achieve a peak SQNR of 117.3dB which meets the requirement of 98dB. Our MSA of -5dBFS also meets the specification (> -6.02dBFS). We achieve a resolution of 19.1 bits.

Now we will briefly compare our simulations to those in the literature (figure A.12 in the appendix). The sweep in the literature has a lower peak SQNR of around 99.2dB but this is to be expected as it was performed at non-ideal conditions. The ideal SQNR at `sinamp` = 0.5 in the literature equals 117.3dB. This matches our simulated SQNR value at `sinamp` = 0.5 of 116.6dB which suggests our simulation is relatively accurate.

7.3 Discussion of Delta Sigma ADC Applications

The ADC designed in this paper [6] is intended to be used in biomedical applications. Common biomedical applications might include implantable devices such as pacemakers and cardiac defibrillators. These devices require incredibly low power consumption. The signals being dealt with in biomedical applications are those extracted from the human body. These are tiny and so we require precise measuring devices with high bit resolution. These biomedical applications tend to have bandwidths in the range of kHz to MHz and in some cases require multi-channel sensors [6].

7.3.1 Why Delta Sigma ADCs are suitable for Biomedical Applications

Firstly, we will discuss why delta sigma ADCs are suitable for this application. One of the key characteristics of delta sigma modulators is oversampling. There are two types of data converters: nyquist-rate and oversampled. Data converters that sample at Nyquist-rate can only achieve a resolution or effective number of bits (ENOB) of $\simeq$ 12. Oversampling at a rate 8 to 512 times higher can allow us to achieve ENOB values up to 20. Since biomedical applications require high precision of up to 16 bits (table 7.1), this makes delta sigma modulators a good choice. The delta sigma modulator in [6] achieves an ENOB of 19.1 according to our simulations. The higher resolution also allows the modulator to process signals from multiple channels at an acceptable bandwidth which is useful for our application. 20 channels are supported by the above design.

Another key characteristic of DSMs is their ability to attenuate noise in the baseband, a process called noise shaping. This allows us to achieve a higher SQNR which will help achieve the system requirement for biomedical applications of 98dB [6].

7.3.2 Why MOD4 CIFF Topology is suitable for Biomedical Applications

Secondly, we will discuss why the MOD4 structure above in particular is suitable for this application. Using a fourth order modulator gives a higher SQNR according to equation 2.1. Additionally, it will reduce the number of clock cycles required to perform a conversion which will allow us to process signals from more channels [6]. By reducing the number of clock cycles, the designers can also increase the bandwidth of the ADC or reduce the sampling rate (f_s) while retaining good SQNR performance.

The 1-bit quantiser removes the need for any DEM scheme as the feedback path will be inherently linear. This significantly simplifies the design and reduces the area cost which is beneficial for biomedical devices that often need to be small. The feedforward architecture (CIFF) is also particularly suitable to biomedical applications. With this structure the input signal is sent directly to the summation point without passing through the integrators. Therefore, the signal distortion generated by the op-amps will not combine with the input signal. This reduces the linearity/ slew rate requirements of the integrators. It also reduces the overall signal distortion which is important when our input signals have small amplitudes as is the case for biomedical applications [6].

Bibliography

[1] Istvan Gyongy University of Edinburgh. *Data Converter Design in Simulink 5, Simulink Design Assignment*. (accessed: 03.04.2022).

[2] Istvan Gyongy University of Edinburgh. *Data Converter Design in Simulink 5, Lab Sheets 1-5*. (accessed: 03.04.2022).

[3] Temes Schreier. *Understanding Delta-Sigma Data Converters*. Wiley-Blackwell, 2004.

[4] Temes Schreier. *THE DELTA SIGMA TOOLBOX Version 7.3*. URL: `https://www.eecis.udel.edu/~vsaxena/courses/ece697A/docs/DSToolbox.pdf`. (accessed: 03.04.2022).

[5] Istvan Gyongy University of Edinburgh. *Data Converter Design in Simulink 5, Lectures 1-10*. (accessed: 03.04.2022).

[6] Antonio W. A. Soares Diomadson R. Belforf Sebastian Y. C. Catunda Raimundo C. S. Freire. *Analysis and System-Level Design of a High Resolution Incremental $\Sigma\Delta$ ADC for Biomedical Applications*. URL: `https://doi.org/10.1145/2800986.2800998`. (accessed: 03.04.2022).

Appendix A

Additional Figures

A.1 Additional Figures from Chapter 2

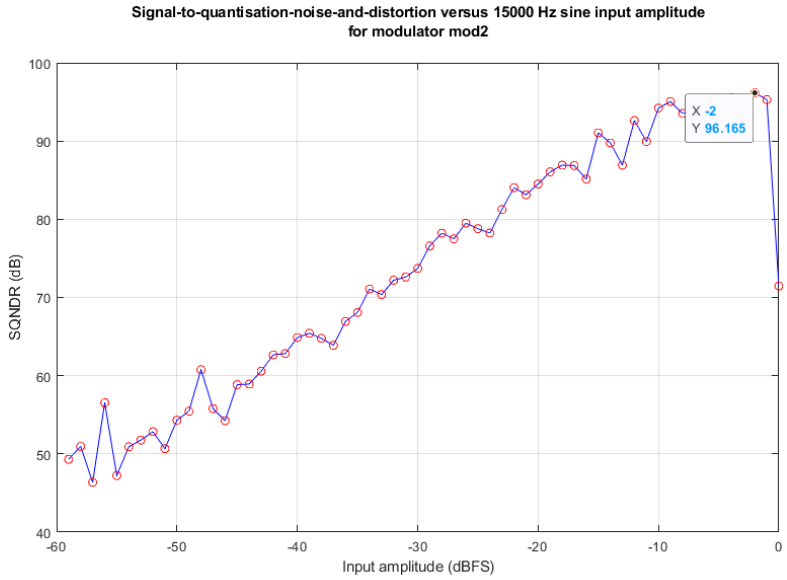


Figure A.1: MOD2 Simulation "sweep_sin_ampl_sqnr" with f_t = 15kHz and OSR 128 with 2-bit quantiser.

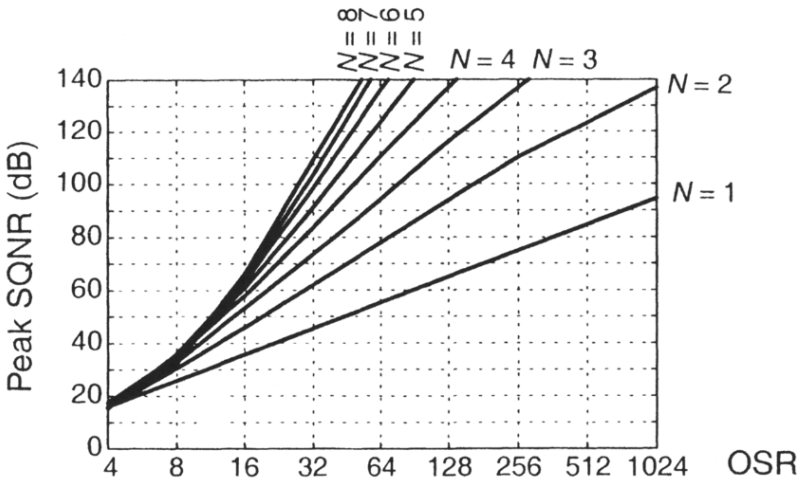


Figure A.2: SQNR vs. OSR for various Modulator Orders, 1-bit quantiser

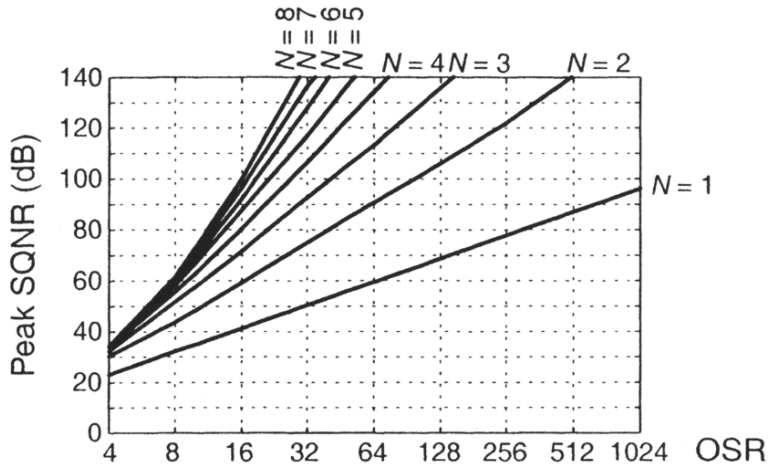


Figure A.3: SQNR vs. OSR for various Modulator Orders, 2-bit quantiser

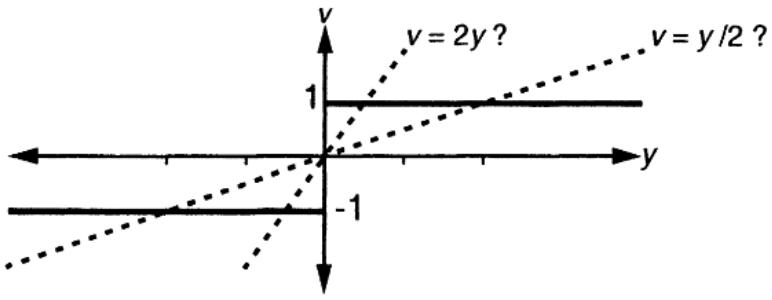


Figure A.4: Gain of a Binary Quantiser is Undefined as there are only Two Levels

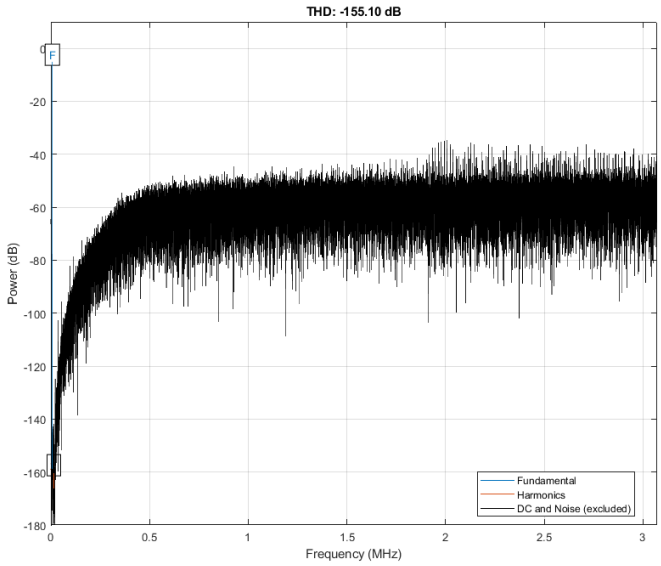
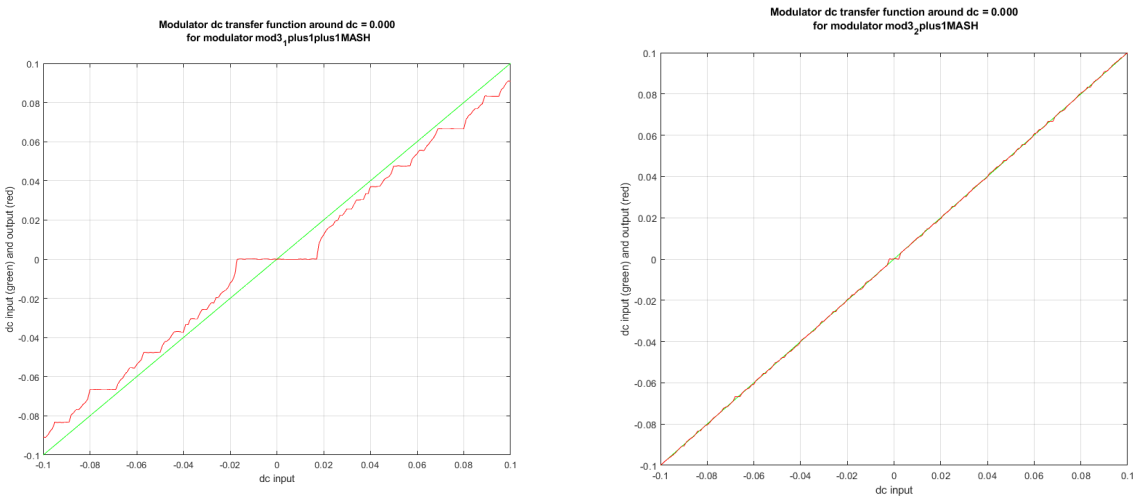


Figure A.5: Total Harmonic Distortion Simulation for CRFF



(a) 1+1+1 Mash Structure

(b) 2+1 MASH Structure

Figure A.6: DC Sweep Simulations, igain = 10 for all Integrators, OSR = 64

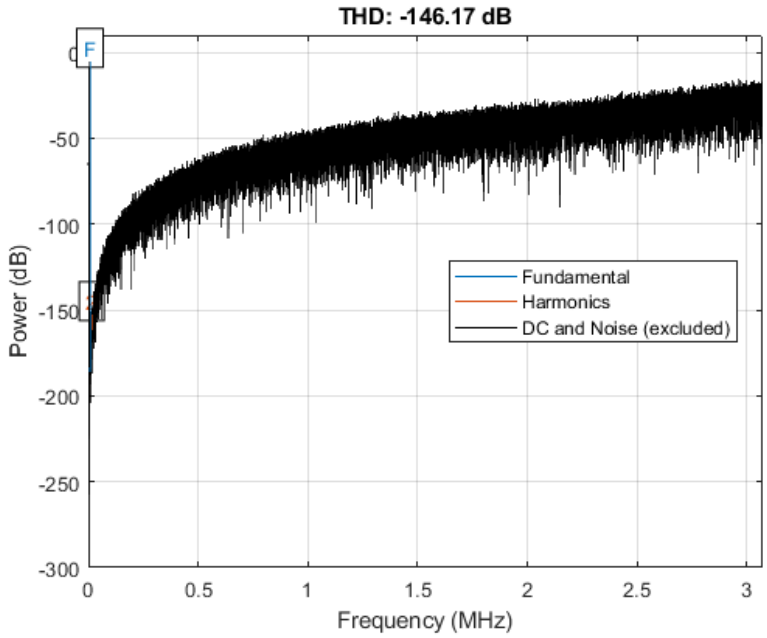


Figure A.7: Total Harmonic Distortion Simulation for MASH 2+1

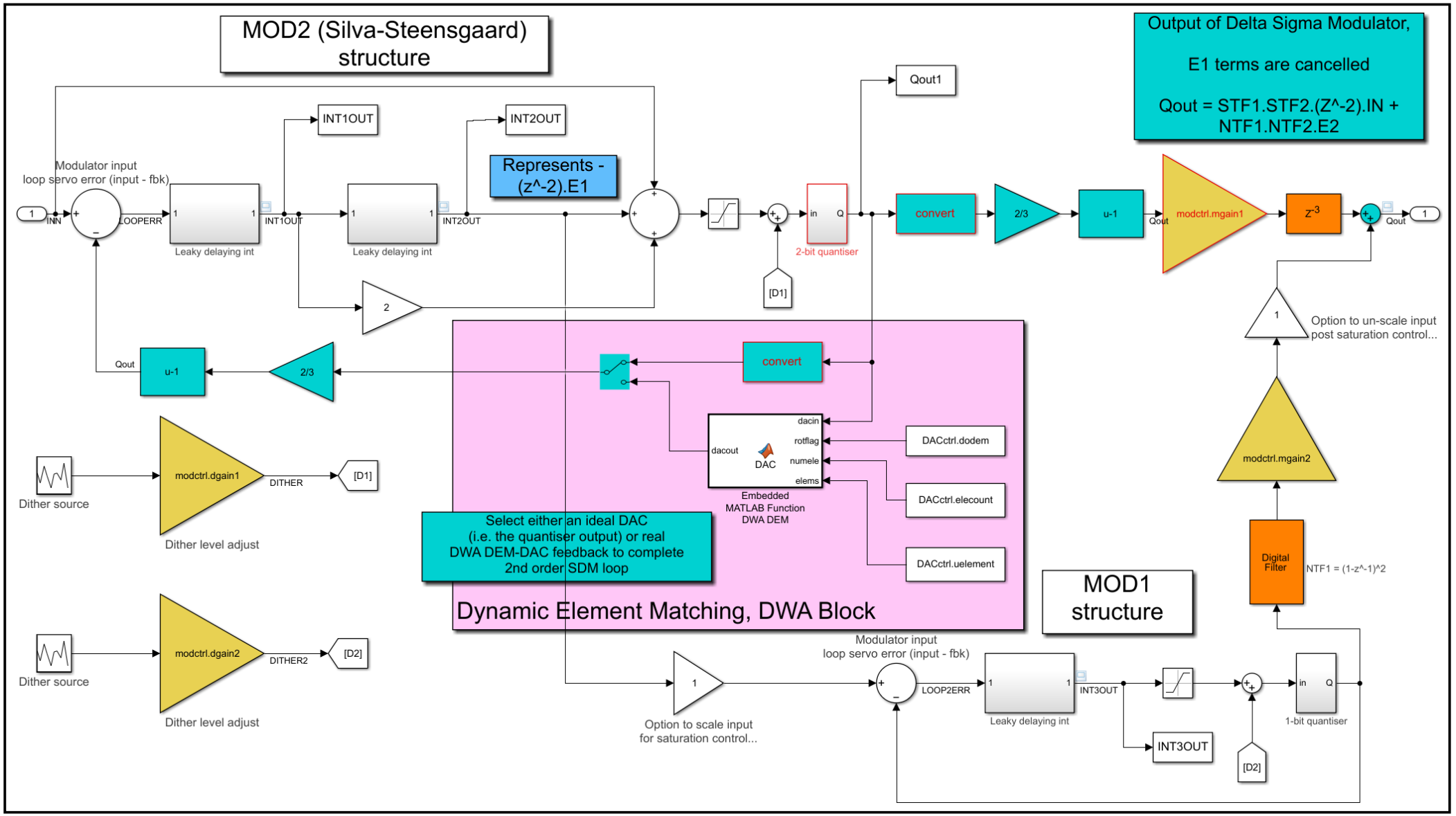


Figure A.8: Schematic of Final MOD3 2+1 MASH Design including DWA DEM-DAC

A.2 Additional Figures from Chapter 3

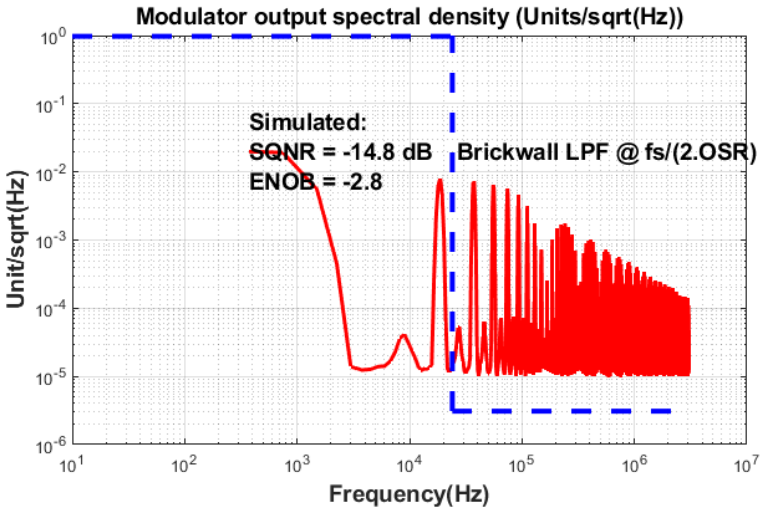


Figure A.9: "Qout_SNDR", `dc_input` = 0.98, Dither = 0.05

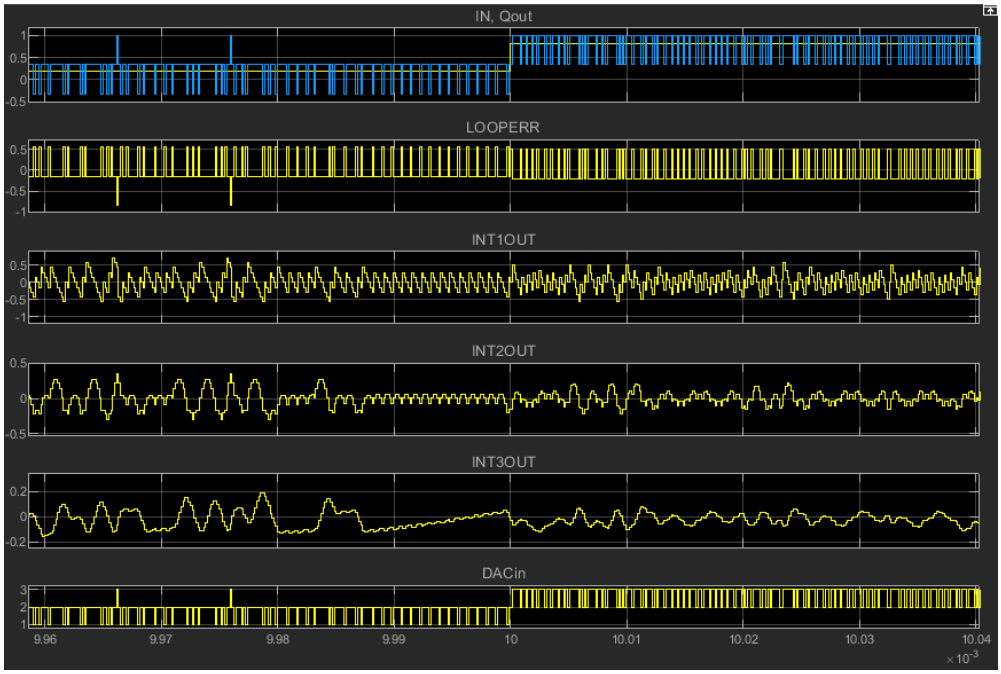


Figure A.10: Time Domain Simulations, Step Input 0.2 to 0.8

A.3 Additional Figures from Chapter 4

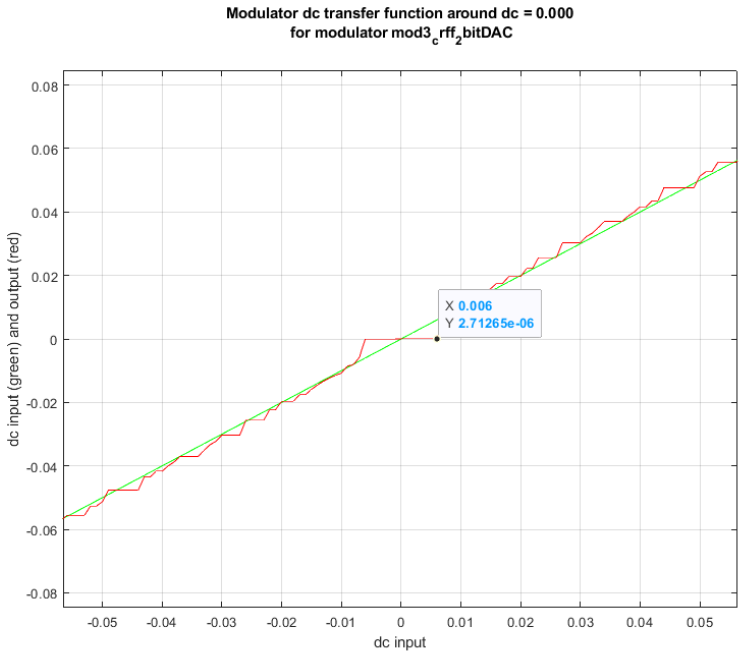
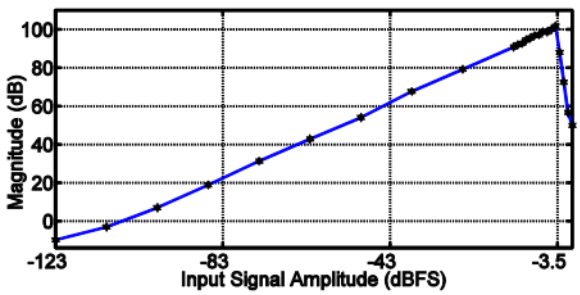
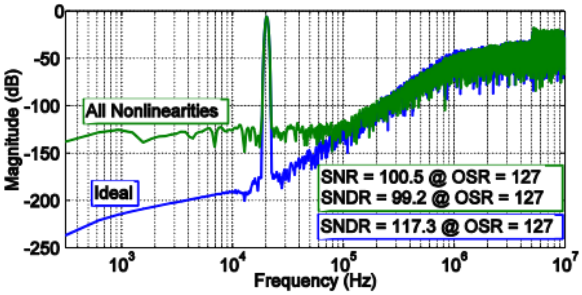


Figure A.11: "sweep_dc_dc", igain = 5 (for all three integrators)

A.4 Additional Figures from Chapter 7



(a) "sweep_sin_ampl_sqnr"



(b) "Qout_SNDR", sinamp = 0.5

Figure A.12: Figures from [6] Showing Modulator Peformance, $f_t = 20$kHz

Appendix B

Additional Tables

B.1 Valid Testing Frequencies

Using the equation below we can calculate all valid testing frequencies. For OSR = 128 we know that $f_s = 6.144$Mhz. N = 8192. The below table has all valid frequencies. We cannot go higher than 20kHz.

$$f_t = \frac{C \times f_s}{N}$$

C	Testing Frequency (f_t)	C	Testing Frequency (f_t)
1	750Hz	14	10500Hz
2	1500Hz	15	11250Hz
3	2250Hz	16	12000Hz
4	3000Hz	17	12750Hz
5	3750Hz	18	13500Hz
6	4500Hz	19	14250Hz
7	5250Hz	20	15000Hz
8	6000Hz	21	15750Hz
9	6750Hz	22	16500Hz
10	7500Hz	23	17250Hz
11	8250Hz	24	18000Hz
12	9000Hz	25	18750Hz
13	9750Hz	26	19500Hz

Table B.1: Valid Testing Frequencies for Modulator with OSR = 128, $f_s = 6.144$Mhz