Technical Report

Analogue Electronics (Project) 4

Summary of Laboratory Results

Final Report

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Statement of Originality

This report, except where otherwise stated through the use of references or acknowledgements is the original work of the author.

Contents

1 Introduction

In this report, the simulation results from three different laboratories will be analysed. Each laboratory explores and compares various circuits of a particular type. In Lab 1 we will look at circuits used for current sensing, which is an important application in the modern world, allowing for technology such as digital photography and biometrics on smartwatches [1]. Lab 2 explores the transmission of digital signals. This is an important topic of discussion as we are often required to send digital signals to other points of our system along PCB tracks or over longer distances using a cable [2]. Finally, in Lab 3 we will cover two methods used for the layout of a mixed-signal chip: manual and automatic, using Cadences's GPDK045 ($45nm$) [3].

2 Current Sensing and Pixel Circuits

2.1 The Photodiode

The photodiode is a widely used current sensor that converts photons into electrons. In order to detect a single electron we require a photodiode capable of single photon detection. Some modern photodiodes such as silicon avalanche photodiodes (APDs) are capable of this. Detecting each individual electron is still difficult since not every photon results in an electron. Electrons can also arise when no photons are present (known as "dark electrons"). There are two main operation modes of a photodiode. In photovoltaic mode the photodiode has zero bias (anode tied to GND). This improves performance in low light (by reducing "dark current"). In photoconductive mode the photodiode is reverse biased. This extends the photodiode's range of linear operation [4].

Since the current of the photodiode is proportional to the absorbed light we can convert the light amplitude into voltage by adding a resistor (R_L) to our photodiode. $V_{DD} = 3.3V$. The photodiode is reverse biased in this configuration. C_{pd} for the photodiode is $11pF$, from our datasheet [5]. Our value of R_L should be as large as possible for maximum V_{out}. $R_{pd} \gg R_L$ should also hold true. We choose $100k\Omega$ since $R_{pd} = 1M\Omega$. i_{pd} is set to $1\mu A$. We should observe an output voltage amplitude of $1\mu A \times 100k\Omega = 0.1V$ or $0.2V$ peak-to-peak. The results are shown in figure 1.

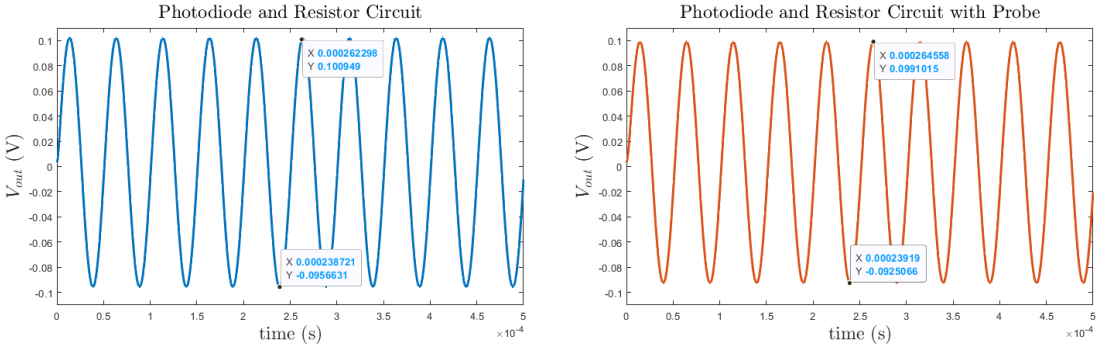


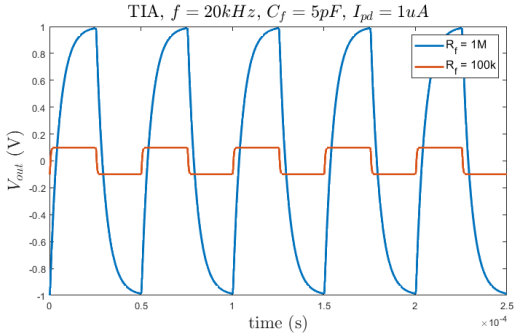
Figure 1: Photodiode Circuit with Resistor recorded V_{out}

The figure on the left shows a peak to peak voltage of just under $0.2V$. If we connect a passive oscilloscope to V_{out} with $10M\Omega$ and $9.5pF$ impedance, we see a reduction in the peak to peak voltage of about $3mV$ shown in the figure on the right. In order to restore this voltage we add a buffer circuit using an "OP_LN" opamp with $I_{bias} = 15\mu A$ and voltage rails $\pm 3.3V$. A schematic of the circuit is shown in figure 18 in the appendix.

2.2 Transimpedance Amplifer (TIA)

The TIA has the same components as the circuit above, but the photodiode is in a different mode of operation. For the TIA, the photodiode is in zero bias mode as the anode is tied to GND.

This reduces "dark current" which improves performance in low light. Figure 1 shows the reverse biased "photodiode with resistor" circuit has a slight offset at low voltages. This problem is not present for the TIA. This also means we ignore R_{pd} as it represents leakage current which is 0 for the TIA. We create the TIA using the "OP_LN" op-amp [6]. It converts current into voltage so we can measure it. A schematic diagram is shown in figure 19. Our initial component values are: $C_f = 5pF$, $R_f = 1M\Omega$, $f = 20kHz$ and pulsed $I_{pd} = 1\mu A$. For any design we want to achieve high stability, bandwidth, sensitivity and gain. Our output should also not saturate. We will have to make trade-offs. The table below shows how altering each component value will effect the output.



(a) Transient Simulation with Initial Values

Saturation↓	$R_f \downarrow$	$C_f \downarrow$	$f \downarrow$
Bandwidth↑	$R_f \downarrow$	$C_f \downarrow$	-
Gain↑	$R_f \uparrow$	-	-
Stability↑	-	$C_f \uparrow$	-
Sensitivity↑	$R_f \uparrow$	-	$f \downarrow$

(b) Effect of Circuit Parameters (TIA)

Figure 2: TIA Initial Simulation at two R_f values and Circuit Parameters Table

Running a simulation with the initial values we find our output is saturated in the transient domain. According to our table we can fix this by reducing our R_f, so we set it to $100k\Omega$. This produces a much better output above in figure 2, but our gain is reduced by 10.

Now lets achieve a higher frequency of $1MHz$. According to our table this will worsen saturation so lets decrease R_f to $1k\Omega$. We will increase I_{pd} to $100\mu A$ so our output is still $0.1V$. This produces the transient simulation in figure 3. However, stability has worsened so we must increase C_f from $5pF$ to $50pF$. We can see the effect this has on stability more clearly in the AC simulation in figure 3. We see no visible peaking at $50pF$. However, we can't increase C_f too much as this will cause saturation (charging too slowly) and a drop in bandwidth which we see at $500pF$.

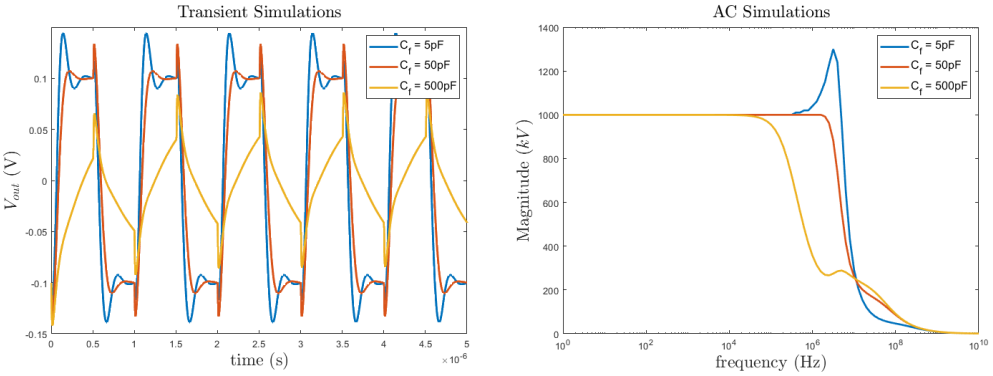


Figure 3: TIA Simulations, $f = 1MHz$, $R_f = 1M\Omega$, $I_{pd} = 100\mu A$

The GBW of this TIA is given in the "OP_LN" datasheet as $2.39MHz$. The value in actual simulations may be different so we create a buffer amplifer circuit to check and find GBW $= 4.8191MHz$. Now we will estimate the expected gain of our TIA when $f = 200kHz$. We require our cutoff frequency to be greater than $200kHz$ which gives us a maximum gain of $1.743M\Omega$.

$$f_c \geq \sqrt{\frac{GBW}{2\pi R_f C_{pd}}} \Rightarrow R_f \geq \frac{GBW}{2\pi {f_c}^2 C_{pd}} = \frac{4.8191MHz}{2\pi(200kHz)^2(11pF)} = 1.743M\Omega \quad (1)$$

Now lets try and measure a very low current of $1nA$. To get an output of $0.1V$ we need to set $R_f = 100M\Omega$. Since R_f is high we have to go to a very low frequency ($f = 200Hz$) to prevent saturation. We run for a number of low C_f (figure 4). By lowering the capacitance to $1pF$ we can remove saturation and achieve a stable square wave output at high sensitivity. We could operate at a higher speed ($2kHz$) but this would require a lower C_f than $1pF$ which is impractical.

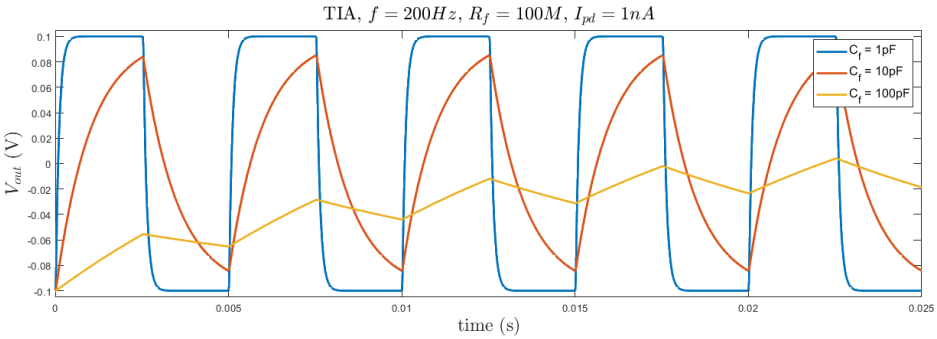


Figure 4: TIA Simulation, $f = 2kHz$, $R_f = 100M\Omega$, $I_{pd} = 1nA$

2.3 Charge Amplifier

In this section we construct and test a charge amp which accumulates charge at the output proportional to I_{in}. A schematic of the charge amp is shown in figure 19 in the appendix. We start with the same initial values as the TIA, $C_f = C_{int} = 5pF$, $f = 20kHz$ ($T_{int} = 25\mu s$), DC current input $I_{in} = 1\mu A$. The gate of the reset transistor V_{pulse} is pulsed from $0 - 5V$. $V_{DD} = 3.3V$. We need to find the appropriate value for C_{int} so we run a simulation sweeping the value (figure 5).

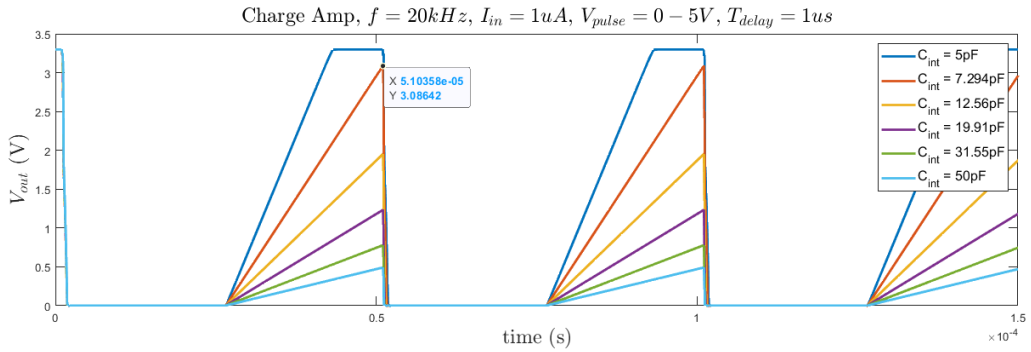


Figure 5: Charge Amp Simulation, $f = 20kHz$, $I_{in} = 1\mu A$, $V_{pulse} = 0 - 5V$, $T_{delay} = 1\mu s$

We see the output saturates for $5pF$. The optimum output occurs when $C_{int} = 7.294pF$. In order to calculate the equivalent transimpedance gain of the charge amplifier, we take the peak V_{out} of our optimum charging curve from the figure above and apply the following formula.

$$gain = \frac{V_{out-peak}}{I_{in}} = \frac{3.0862V}{1\mu A} = 3.086 \times 10^6 \tag{2}$$

Now lets look at the relationship between gain and the circuit parameters. We can see from figure 5 that as C_{int} increases, gain decreases, as charging is slower (inversely proportional). Furthermore, as frequency (f) increases or T_{int} decreases, gain decreases as there is less time for the amplifier to charge each cycle. Table 1 shows the relationship between gain and T_{int}/f in simulations.

Finally we will try to measure a very low current of $10pA$ using longer integration times (lower frequency). We will try a very high $500ms$ period ($f = 2Hz$, $T_{int} = 250ms$) with various C_{int} to see if this will give us enough time to charge to a reasonable level. The result is shown in figure 6.

A good peak voltage of $2.17V$ is achieved with $C_{int} = 1pF$. We could use a lower T_{int} with a lower capacitance $(0.1pF, 0.5pF)$ but, as with the TIA, this may not be practical as these capacitors are tricky to source and parasitic capacitance may also be larger than this.

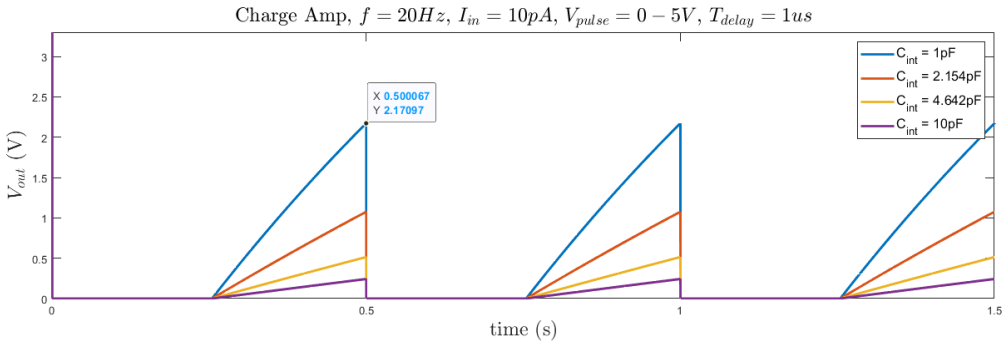


Figure 6: Charge Amp Simulation, $f = 2Hz$, $I_{in} = 10pA$, $V_{pulse} = 0 - 5V$, $T_{delay} = 1\mu s$

2.4 Active Pixel Sensor (APS)

While the performance of the TIA above is good as a photodiode readout circuit, it is impractical due to its size. Therefore, we build an active pixel sensor (APS). First we model a simple source follower using two NMOS. $V_{DD} = 5V$. To find the appropriate value for V_{bias} we run DC simulations of V_{out} against V_{in} for a number of different V_{bias} and observe the output (figure 20 in the appendix).

We need our NMOS to operate in saturation mode, so we require $V_{bias} \geq V_{th}$ and $V_{out} \geq V_{bias} - V_{th}$. Using Cadence results browser we find $V_{th} = 0.7525V$. Therefore, we choose $1V$ as a good V_{bias} point. We complete the APS by adding a PMOS reset switch and a photodiode, modelled by a current source/ capacitor ($C_{pd} = 22$nF). V_{reset} is a pulsed square wave source. We need to switch the PMOS between linear mode (on) and cut-off mode (off). Therefore, according to the PMOS equations, we pulse V_{reset} between $0-5V$. We set the period of V_{reset} to 10ms (pulse width = 5ms). We run a transient simulation and plot V_{out} for various I_{pd} values. This produces figure 7 below.

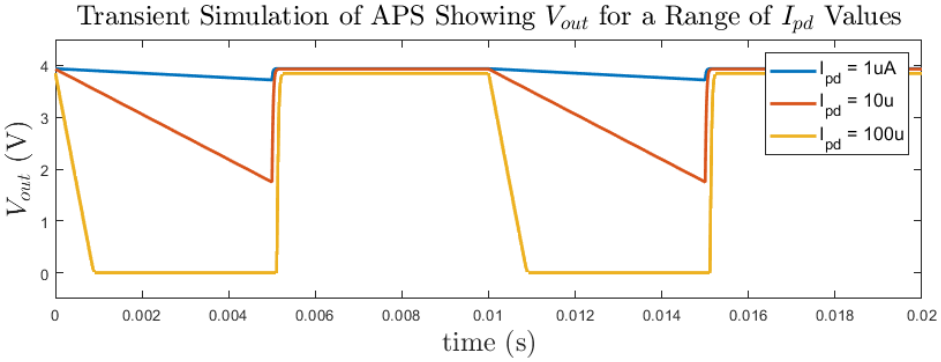


Figure 7: Transient Simulation of 3T APS Showing V_{out} for a Range of I_{pd} Values

Charge begins to accumulate on the capacitor C_{pd} at time = 0ms. The pulse width or exposure time is 5ms. We read the pixel value just before reset. The lower light amplitude ($I_{pd} = 1\mu A$) requires a longer exposure time to be properly measured. $I_{pd} = 10\mu A$ is at approximately the right level. In the case of $I_{pd} = 100\mu A$, the pixel has saturated, which means the light is too high and the measurement is invalid. Higher currents need shorter V_{reset} periods (integration time).

There are a few ways we can avoid saturation in active pixel sensors. One method is to use a shorter exposure time so saturation does not have time to occur. Additionally, the charging constant for a capacitor $\tau = RC$. Therefore if we increase C_{pd}, discharging will take more time. This

will decrease the discharge slope seen in figure 7 and prevent saturation. Currently we are using a PMOS for our reset switch which takes up more space than an NMOS. To decrease the size of the pixel it would be beneficial to switch to an all NMOS 3T APS. This is possible but through simulation we learn it does result in a drop in the peak value of V_{out} to $\simeq 3V$ (see figure 21 in the Appendix). This makes sense as the NMOS has a higher on-resistance.

2.5 High Dynamic Range (HDR) pixel

2.5.1 Unlimited Dynamic Range

Saturation limits the dynamic range of our pixel sensor but there are solutions. We know the discharge slope is proportional I_{pd}. Therefore, we can read the discharge slope of a saturated output and still find I_{pd}. To measure the slope we add a comparator "COMP" to our APS [7]. When the discharge slope passes a threshold voltage (V_{th}) near to $0V$, say $100mV$, the comparator will be triggered. The time at which the comparator is triggered (t_1) is recorded. The start time is t_0. Therefore we can find the discharge slope using the following equation.

$$slope = \frac{V_{peak} - V_{th}}{t_1 - t_0} \tag{3}$$

The full APS schematic is shown in figure 22. Figure 8 shows V_{out} and the output of the comparator (V_{comp}) for a range of I_{pd} values. We can now calculate I_{pd} from the output of the comparator.

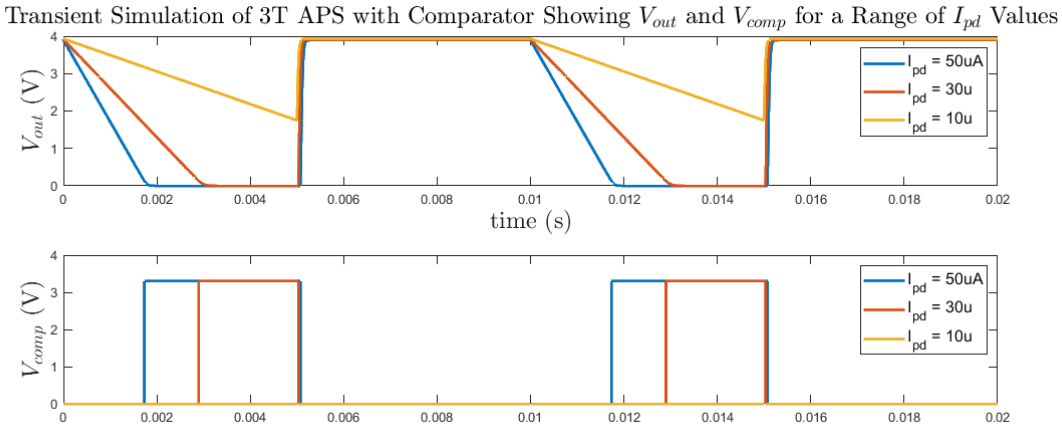


Figure 8: Simulation of 3T APS Showing V_{out} and V_{comp} for a Range of I_{pd} Values

For $50\mu A$, $t_1 = 1.73ms$, $t_0 = 0ms$, $V_{peak} = 3.69V$ and $V_{th} = 100mV$. This gives a slope according to equation 3 of 2075.14. According to the time constant equation we know that $R = \frac{V}{I} = \frac{\tau}{C}$. Rearranging, $I = \frac{V}{\tau} \times C = slope \times C$. Therefore, $I_{pd} = 2075.14 \times 22nF = 45.6\mu A$. This is close to the actual $50\mu A$. This method of reading the value of the pixel has increased our dynamic range.

2.5.2 Dual Integration

Comparators take up too much space to be used in real circuits. Therefore, to improve dynamic range we utilise dual integration. We perform two sequential integrations with different periods. The shorter V_{reset} pulse measures the higher currents before they saturate and the longer pulse can measure lower currents. Applying dual integration to our circuit we produce the output shown in figure 9 for integration times of $5ms$ and $50ms$.

For the shorter integration time only the 2 largest currents are saturated which is improved from the longer integration time. We can sample the smallest current of $1\mu A$ at the end of the longer integration time. This is better than measuring at the end of the smaller time because the voltage

drop is bigger. Thus any measurement errors will have a smaller impact on overall accuracy of the APS. Creating a high dynamic range is difficult as it is challenging to build a solution that will work for a large range of currents. In this case, two of the currents remain saturated.

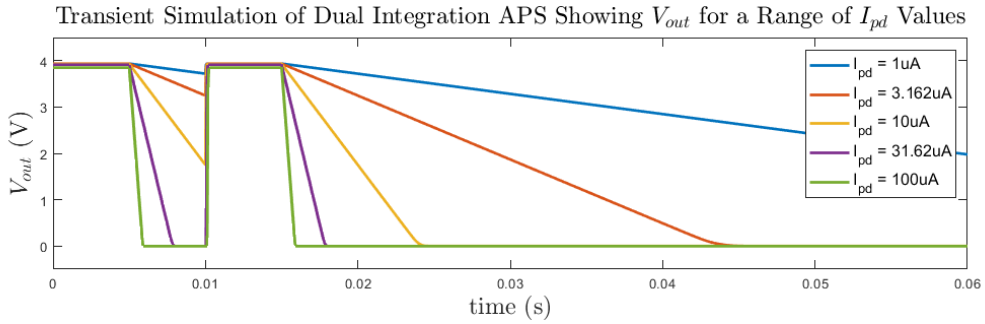


Figure 9: Simulation of Dual Integration APS Showing V_{out} and V_{comp} for a Range of I_{pd} Values

3 Digital Signalling

Digital signalling is made up of a transmitter (TX), receiver (RX) and transmission line. This transmission line can introduce losses and imperfections to the digital signal. We will now simulate some different digital signalling circuits and compare them. We will also consider the effect of power supplies having finite impedance.

3.1 CMOS Logic

In this section we investigate the push-pull inverter, a building block of CMOS circuits. A schematic is shown in figure 23 in the appendix. M1 and M2 represent our transmitter, M3 and M4 are the receiver. The transmission line between TX and RX is modelled by $R_L = 2k\Omega$ and $C_L = 10nF$. First we will observe how our outputs change with increasing frequency. Results are shown in figure 10 below. Our input V_{in1} is a pulsed waveform between $0 - 5V$.

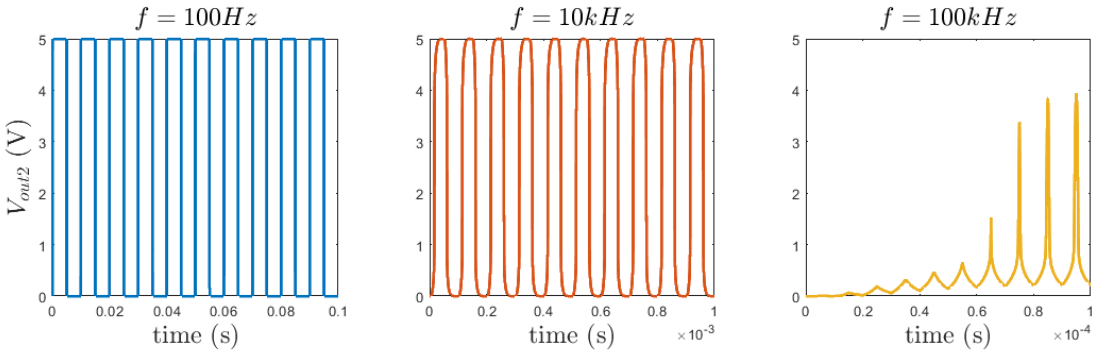


Figure 10: CMOS Push-Pull Inverter V_{out2} at Various Input Frequencies

At low frequencies such as $100Hz$ we see perfect replication of the input waveform. R_L and C_L form a LPF which will begin to attenuate our signal at $7.957kHz$ according to the formula for cutoff frequency ($f_c = \frac{1}{2\pi R_L C_L}$). Therefore, at $10kHz$ we begin to see issues with our output in figure 10. At $f = 100kHz$ we observe complete breakdown. We no longer receive a proper signal at V_{out2}. If we define our frequency limit as the frequency before the first pulse completely collapses then $f_{max} \simeq 30kHz$. At this point the output is not replicating the input accurately. As we decrease R_L and C_L this limit frequency will increase and our output will no longer be attenuated at $100kHz$. This is illustrated by the two simulations in figure 11 below which show V_{out2} at $100kHz$ for various capacitor and resistor values. Performance improves at lower values.

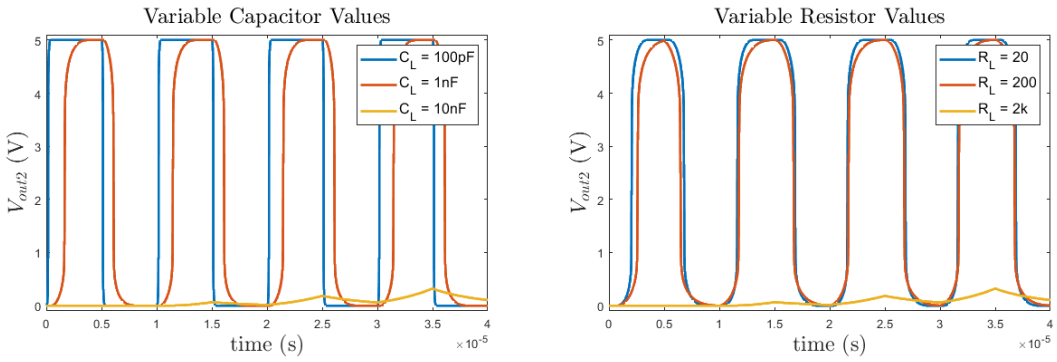
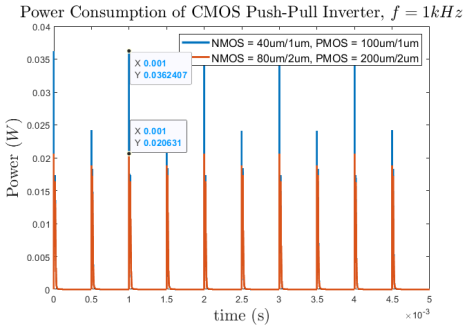


Figure 11: CMOS Push-Pull Inverter V_{out2}, $f = 100kHz$

Now we will examine the average power (P_{avg}) and peak power (P_{peak}) consumption of this circuit per edge transition by plotting "pwr" in the Cadence results browser (figure 12). We observe as frequency increases, P_{avg} increases but our peak power is the same. We calculate power consumption for different sized transistors. Larger transistors can allow us to achieve a higher frequency limit but they also result in higher peak power consumption (P_{peak}).



(a) Power Consumption, $f = 1kHz$

	NMOS = $40\mu m/1\mu m$ PMOS = $100\mu m/1\mu m$		NMOS = $80\mu m/2\mu m$ PMOS = $200\mu m/2\mu m$	
f	P_{avg}	P_{peak}	P_{avg}	P_{peak}
$10Hz$	$5.392\mu W$	$20.63mW$	$5.506\mu W$	$36.24mW$
$100Hz$	$53.92\mu W$	$20.63mW$	$55.06\mu W$	$36.24mW$
$1kHz$	$539.2\mu W$	$20.63mW$	$550.\mu W$	$36.24mW$
$10kHz$	$4.997mW$	$19.68mW$	$5.117mW$	$35.09mW$
$100kHz$	$7.589mW$	-	$7.799mW$	-

(b) Table of Power Consumption

Figure 12: Power Consumption of CMOS Push-Pull Inverter, $C_L = 10nF$, $R_L = 2k\Omega$

Finally, we look at the effect of adding a finite resistance of 50Ω to VDD. For $f = 1kHz$, by probing V_{DD} we see that each transition causes a negative spike in the voltage. From $5V$ to $4.87V$ on the rising edge and $4.79V$ on the falling edge. The switching causes the current and power consumption to spike as shown in figure 12. This creates a voltage drop across the resistor.

3.2 Current Mode Logic (CML)

CML has a differential configuration as shown in the schematic diagram in figure 24. Differential signalling has many benefits. First we will examine the voltages at various frequencies, as we did for the push-pull inverter. $R_L = 1k\Omega$, $C_L = 10nF$, $RP = RN = 1k\Omega$. This time our V_{in} is a pulse from $0 - 3.3V$ and $V_{DD} = 3.3V$. The results are shown in figure 13.

At $10kHz$ we observe perfect replication of the input which is better than the CMOS inverter (figure 10). At $100kHz$ it takes a number of pulses for the output to settle. There is also a time offset between the input and output. It is difficult to define a maximum frequency as even at very high frequencies ($1M\Omega$), after a long enough settling time, V_{out2} will replicate the input pulse. Defining the frequency limit as the frequency that requires no longer than 10 pulses to produce an output, we calculate $f_{max} \simeq 200kHz$. This is much larger than for our push-pull inverter above. Similar to the push-pull inverter, decreasing R_L and C_L values improves our output at higher frequencies, leading to shorter settling times. Now we examine the power consumption of our circuit by plotting "pwr" for various frequencies (figure 14). We find P_{avg} by averaging the transient

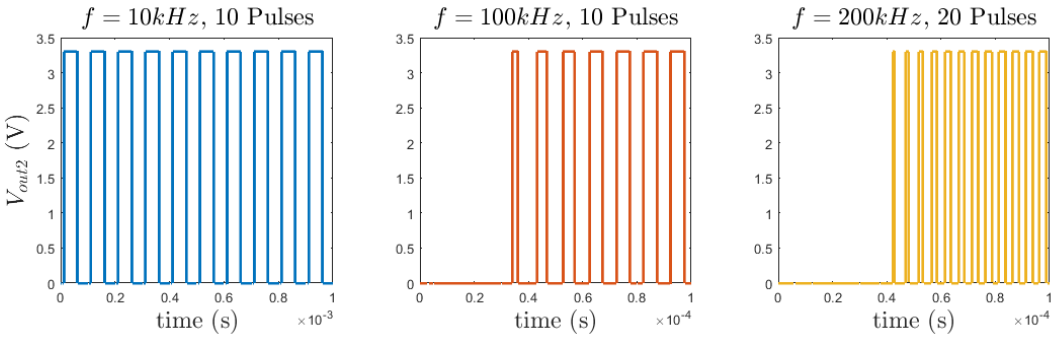
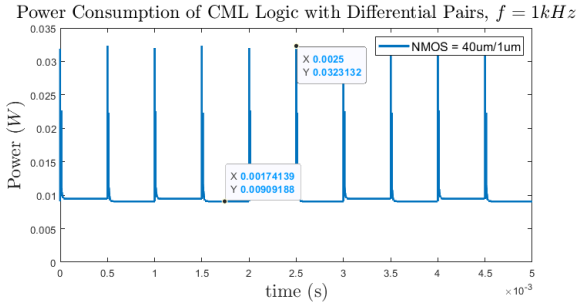


Figure 13: CML Logic with Differential Pairs V_{out2} at Various Input Frequencies

plot of power consumption. P_{peak} is the maximum power consumed on the transition edge. For the CML logic, the power consumption is $\simeq 9mV$ when a transition is not occurring compared to $\simeq 0mV$ for the CMOS push-pull inverter. This increases P_{avg}. The peak power is also higher.



(a) Power Consumption, $f = 1kHz$

f	P_{avg}	P_{peak}
$10Hz$	$9.285mW$	$32.2893mW$
$100Hz$	$9.296mW$	$32.2968mW$
$1kHz$	$9.413mW$	$32.3132mW$
$10kHz$	$10.48mW$	$31.7488mW$
$100kHz$	$11.8mW$	-

(b) Table of Power Consumption

Figure 14: Power Consumption of CML Logic with Differential Pairs

We now look at the power consumed by the TX unit at $f = 1kHz$. We plot the "pwr" of each component of the transmitter module using the Cadence Results Browser: $M1$, $M2$, $M3$, RP and RN. This is shown in figure 25 in the appendix. The lowest peak power (P_{peak}) we can get away with for the CML TX is $\simeq 16.39mW$ (maximum power consumed by the TX at any one time).

We have shown that compared to the CMOS configuration, CML has a much higher power consumption which is undesirable. When we give V_{DD} a finite impedance of 50Ω we see a drop in voltage from $3.3V$ to $3.01V$ at each transition. This is worse than the drop observed for CMOS. Furthermore, for CMOS the voltage only dropped at the transition edges, but for CML the voltage drops down to $3.16V$ even when a transition is not occurring. Plots of V_{DD} for CML and CMOS with finite impedance 50Ω are shown in figure 26. If I was choosing a circuit for digital signalling I would select the CML, due to its better performance at high frequencies. However, CMOS does have better power consumption and lower susceptibility to finite power supply impedance.

3.3 Signal Integrity & Transmission Lines

Previously, we assumed a simple RC model for the transmission line which is suitable for lower frequencies and slow rise/fall times. Now we will use an RLC circuit to model the line. We make the circuit shown in figure 27 with a TX inverter, transmission line and termination load. $R_{TL} = 0.1\Omega$, $L_{TL} = 250nH$, $C_{TL} = 100pF$ and $R_L = 1M\Omega$. We set a sharp rise/ fall time ($1ps$). Now we simulate V_{out1} and V_{out2} (before/ after the transmission line). V_{in} is pulsed between $0-5V$. We simulate a simplistic "lumped" RLC model. We also model each section of the transmission line with a separate RLC model. For this, we divide the RLC values used above by N (the number of divisions). We set $N = 10$ and $N = 100$. All the results are shown in figure 15 below.

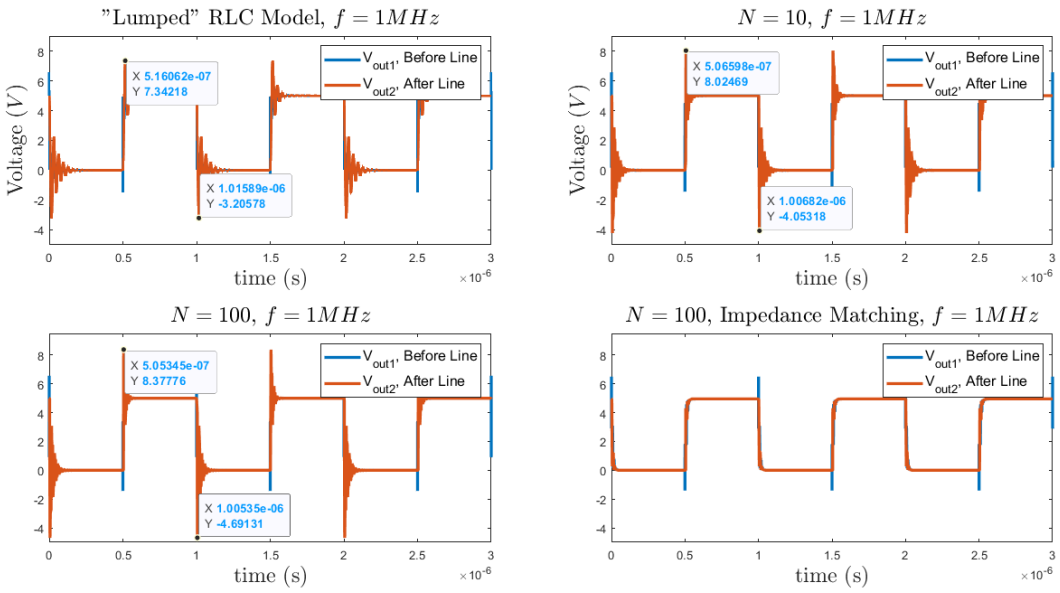


Figure 15: Simulation of TX Inverter with "Lumped" and Distributed RLC Models

Impedance mismatch results in reflections down the line causing distortion of the outputs. This distortion is higher for the more accurate distributed RLC Models. As we increase N, the distortion increases. To fix this we must match the impedances. We find the R_{out} of the inverter and add a resistor (R_M) between TX and the transmission line to cover the difference between R_{out} and the line impedance. We also choose R_L to match the line impedance. We set $R_M = 70\Omega$, $R_L = 10k\Omega$. This gives the fourth plot in figure 15. We can see the distortion at V_{out2} has been removed.

4 Manual vs Automatic Layout

4.1 Manual Layout

In this section we implement a 3 gate logic circuit using manual layout. The logic table is shown in table 2. The final manual layout is shown in Figure 30 in the appendix. We perform a simulation on both the pre-layout and post-layout circuits. Inputs "a" and "b" are both pulsed with different periods to create a rolling offset. 7ns is used for "a" and 9ns is used for "b". The simulations are run for $\simeq 20$ pulses. $V_{DD} = 1V$. This produces the outputs shown in figure 16 below.

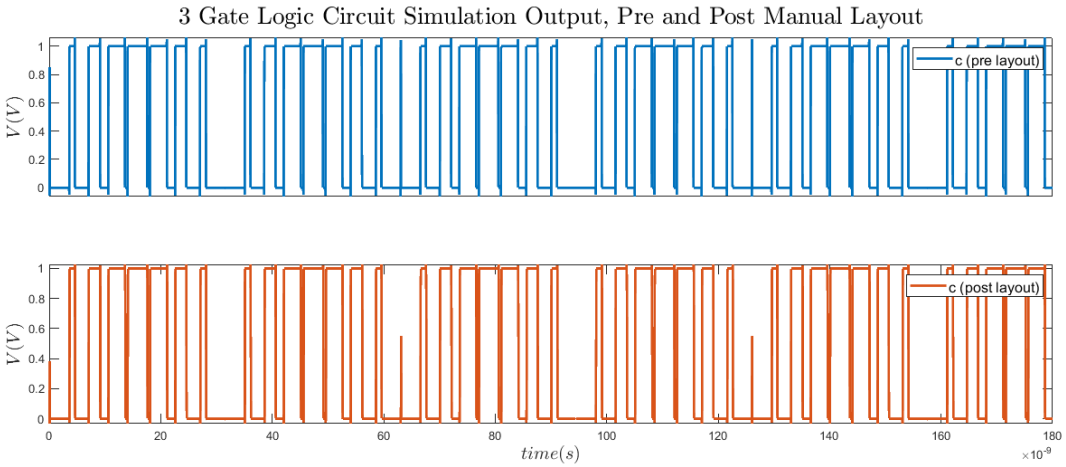


Figure 16: Simulation Outputs of Three Gate Logic Circuit (Pre/ Post Layout)

When the two inputs are the same, $c = 0$ and when they are different $c = 1$. Comparing the two outputs, pre-layout has more visible peaking which would indicate higher levels of parasitic capacitance. The post-layout takes longer to transition from high to low and vice-versa due to a higher delay. This is more visible in figure 28 in the appendix. Occasionally, a very short output pulse is triggered by inputs "a" and "b". Due to the additional delay, the post-layout output cannot pulse fully and only reaches $\simeq 0.5$V. This effect is most obvious at $\simeq 64$ns and $\simeq 125$ns.

4.2 Automatic Layout

Now we will implement the layout of a 4-bit `counter.v` verilog file automatically. The completed automatic layout is shown in figures 31 and 32 in the appendix. We simulate the output of the counter pre and post-layout. The output is a 4-bit count. Running a transient simulation for $10ns$ with the clk period set to $1ns$ ($f = 1GHz$) we produce the outputs in figure 17.

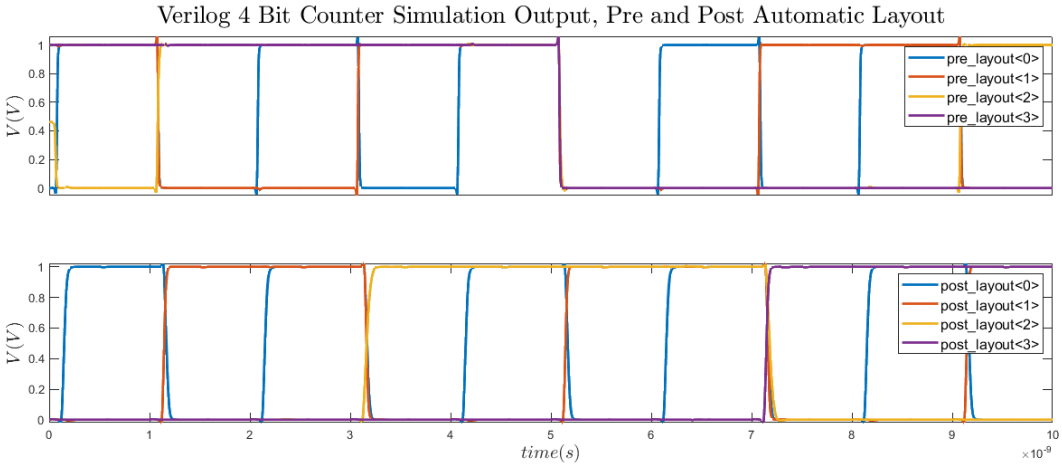


Figure 17: Simulation Outputs of 4-bit Verilog Counter (Pre/ Post Layout)

We observe that the pre-layout counter output starts with some of the bits of the counter set to 1. This could be evidence of extra parasitic capacitance present in the pre-layout, which is causing some of the outputs to be driven high at the start of the simulation. Similar to the manual layout simulation we see increased peaking for the pre-layout output. The post-layout simulation also has a longer delay when transitioning. This is more visible in figure 29 in the appendix.

The maximum frequency pre and post-layout was calculated by running transient simulations with the clk period set to increasingly shorter periods. The max frequency was defined as the highest frequency where the counter still changes by 1 every clk cycle. It was found to be $\simeq 3.22$GHz (310ps period) for post-layout and $\simeq 5.88$GHz (170ps period) for pre-layout. The pre-layout counter has a higher max frequency as it has a shorter delay when changing between logic levels.

5 Conclusion

This report has examined the performance of a wide range of common current sensing circuits. We simulated a TIA and a Charge Amplifer, concluding that due its size the TIA is not usable in many modern day applications such as digital photography. We analysed the performance of an APS and discussed various HDR methods. In regard to digital signalling, we concluded that while CML performs better at higher frequencies, CMOS logic has much lower power consumption and lower susceptibility to finite V_{DD} impedance. We also saw the importance of impedance matching in transmission lines. Finally, we looked at manual and automatic layout techniques. By simulating circuits pre and post layout we saw the superior performance of post layout circuits and why implementing optimum layouts for mixed-signal chips is important in modern design processes.

References

[1] The University of Edinburgh Danial Chitnis. *Laboratory 1, Current Sensing And Pixel Circuits, Lab book*. (accessed: 07.04.2022).

[2] The University of Edinburgh Danial Chitnis. *Laboratory 2, Digital Signalling, Lab book*. (accessed: 07.04.2022).

[3] The University of Edinburgh Danial Chitnis. *Laboratory 3, Manual vs Automatic Layout, Lab book*. (accessed: 07.04.2022).

[4] All About Circuits Robert Kiem. *Understanding Photovoltaic and Photoconductive Modes of Photodiode Operation*. URL: `https://www.allaboutcircuits.com/technical-articles/understanding-photovoltaic-and-photoconductive-modes-of-photodiode-operation/`. (accessed: 07.04.2022).

[5] OSRAM Opto Semiconductors. *Radial T1 3/4, SFH 203 P Silicon Pin Photodiode Datasheet*. URL: `https://www.osram.com/ecat/Radial%20T1%203-4%20SFH%20203%20P/com/en/class_pim_web_catalog_103489/prd_pim_device_2219552/`. (accessed: 07.04.2022).

[6] AMS. *Analog Standard Cell OP_LN – CMOS Operational Amplifier*. URL: `https://en.sekorm.com/doc/2398032.html`. (accessed: 07.04.2022).

[7] AMS. *Analog Standard Cell COMP – CMOS Comparator*. URL: `https://en.sekorm.com/doc/2396440.html`. (accessed: 07.04.2022).

A Supplementary Figures

A.1 Additional Figures from Lab 1

These consist of non essential schematic diagrams and additional plots which have been added for further clarification and detail.

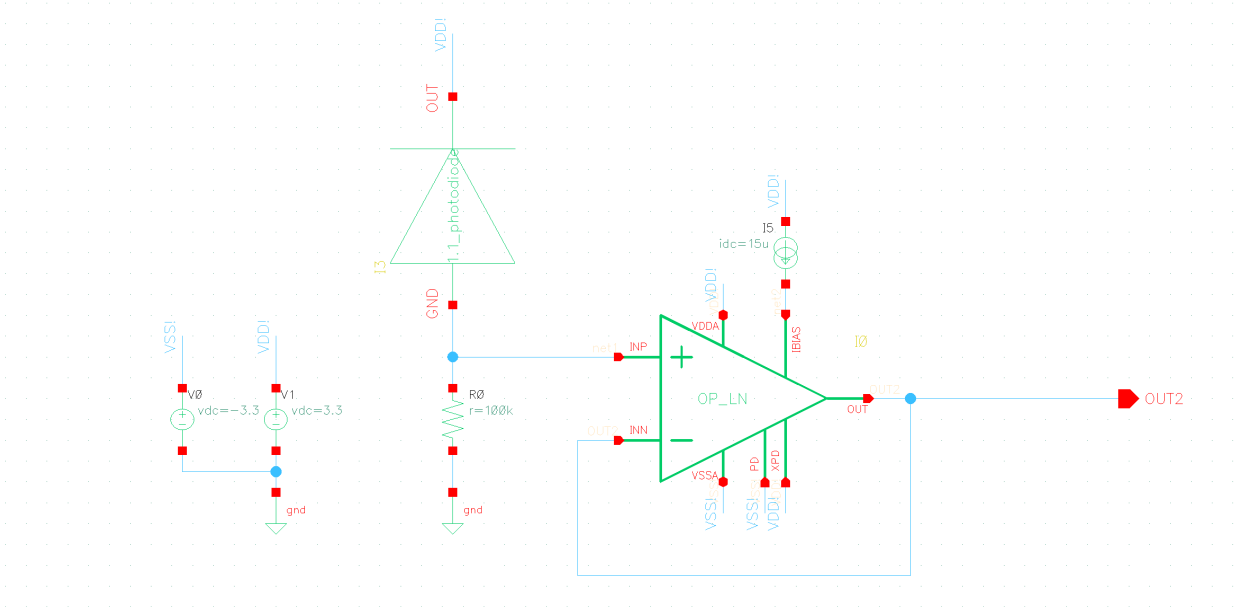
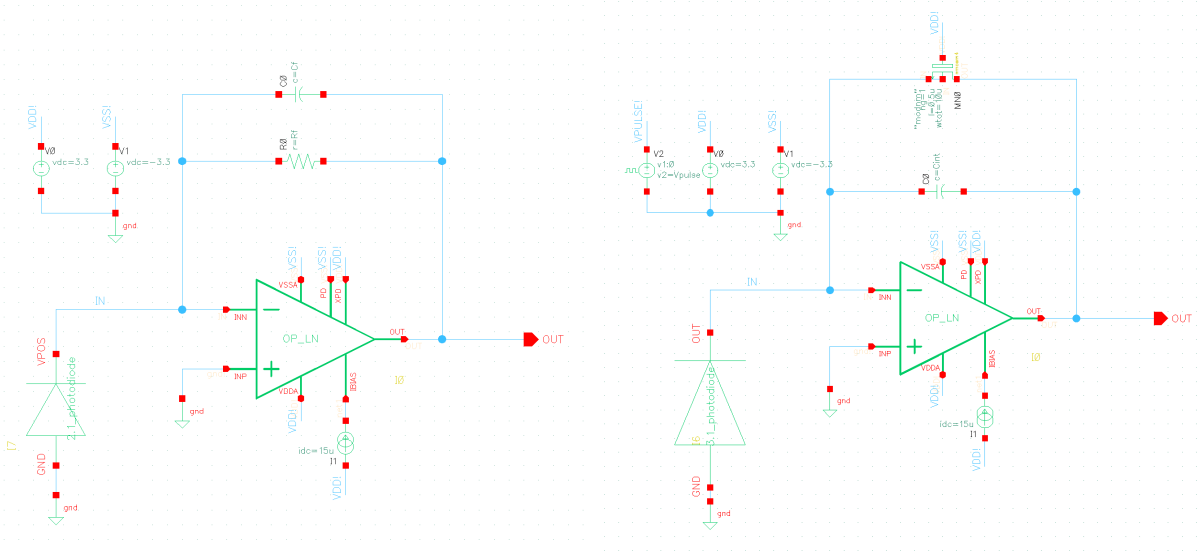


Figure 18: Schematic Diagram of Photodiode and Resistor Circuit with Buffer Op-Amp



(a) Transimpedance Amplifier (TIA)

(b) Charge Amplifier

Figure 19: Schematic Diagrams from Lab 1

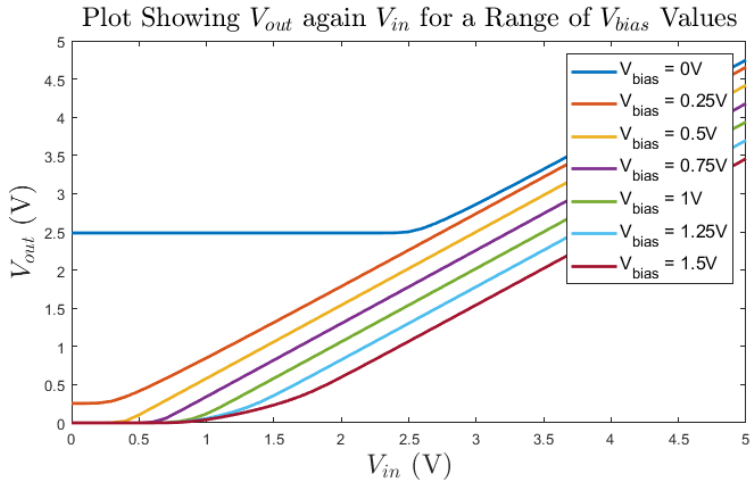


Figure 20: DC Simulations of V_{out} vs V_{in} for various V_{bias} values.

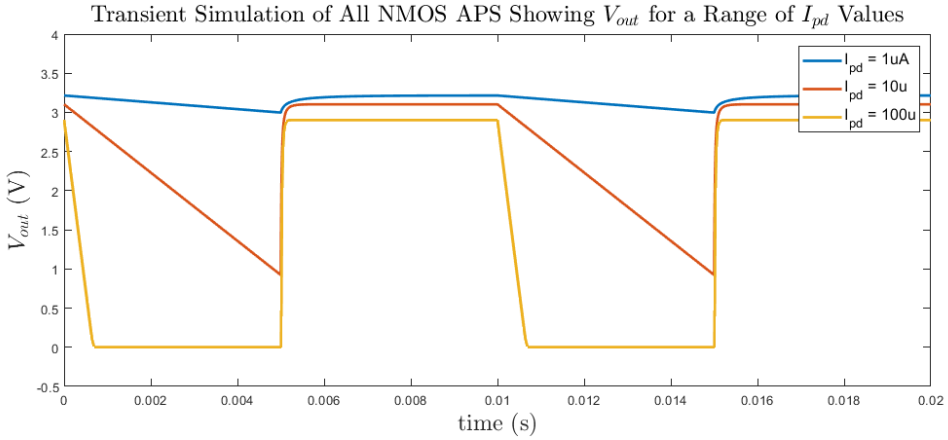


Figure 21: Transient Simulation of All NMOS 3T APS Showing V_{out} for a Range of I_{pd} Values

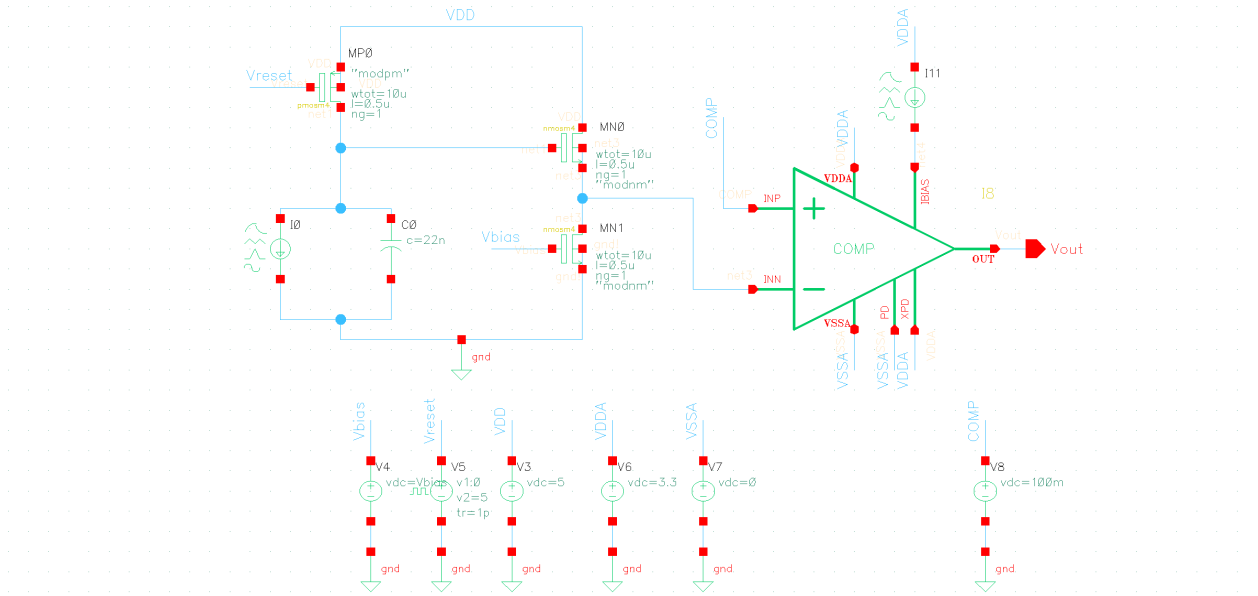


Figure 22: Schematic Diagram of 3T Active Pixel Sensor with Comparator

A.2 Additional Figures from Lab 2

These consist of non essential schematic diagrams and additional plots which have been added for further clarification and detail.

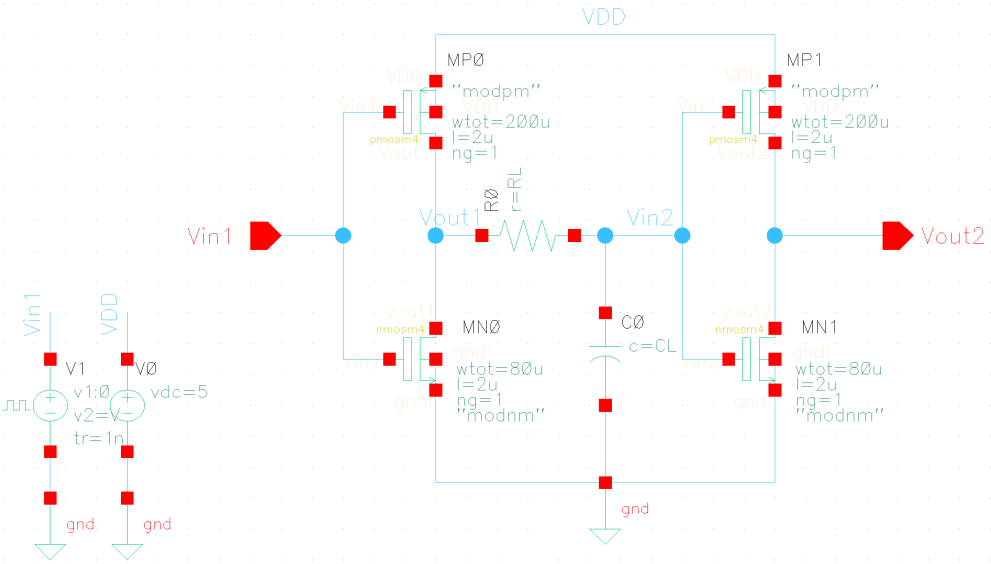


Figure 23: Schematic Diagram of CMOS Push-Pull Inverter

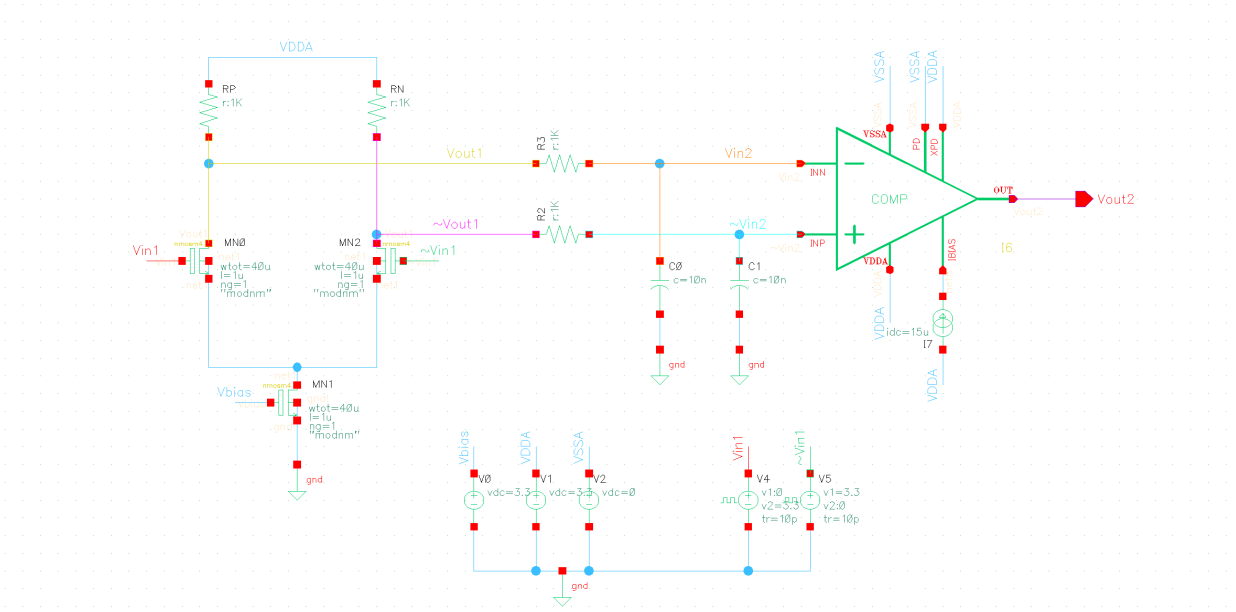


Figure 24: Schematic Diagram of CML Logic with Differential Pairs

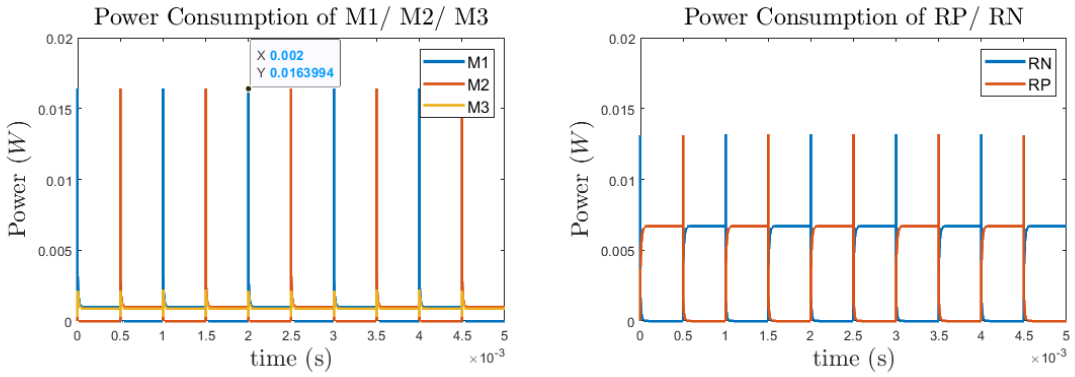


Figure 25: Power Consumption of TX Unit of CML Logic, $f = 1kHz$

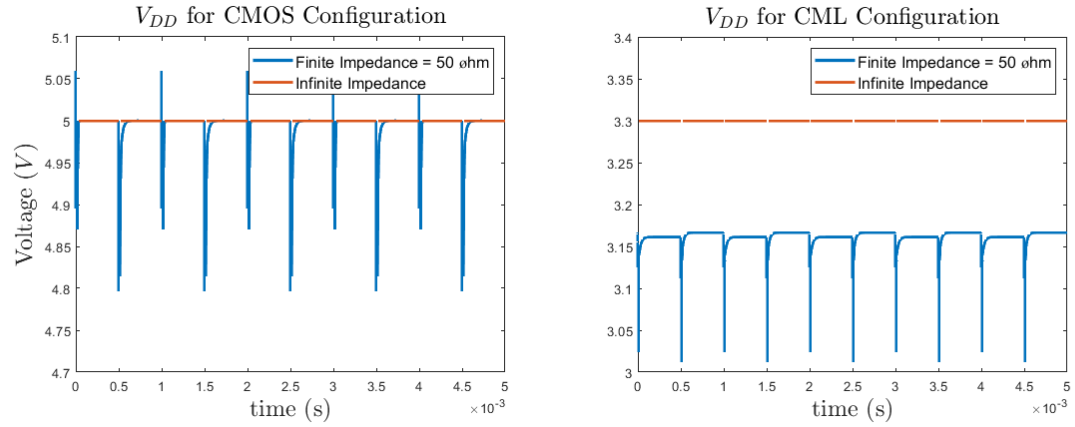


Figure 26: Transient Plot Showing V_{DD} with and without Finite Impedance of 50Ω

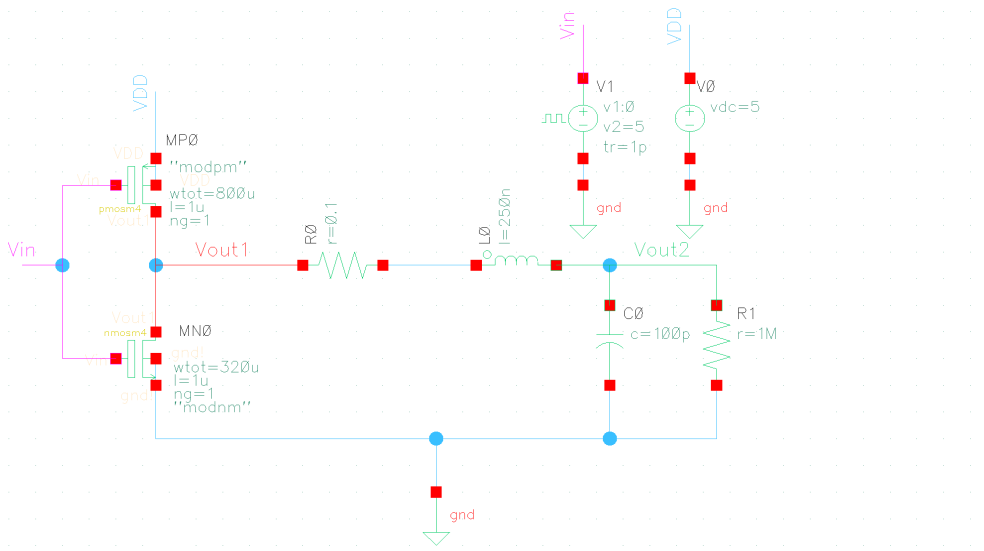


Figure 27: Schematic Diagram of TX Inverter, with "Lumped" RLC Transmission Line Model and Termination Load

A.3 Additional Figures from Lab 3

This subsection includes additional plots as well as full page schematics of the manual and automatic layouts from Lab 3.

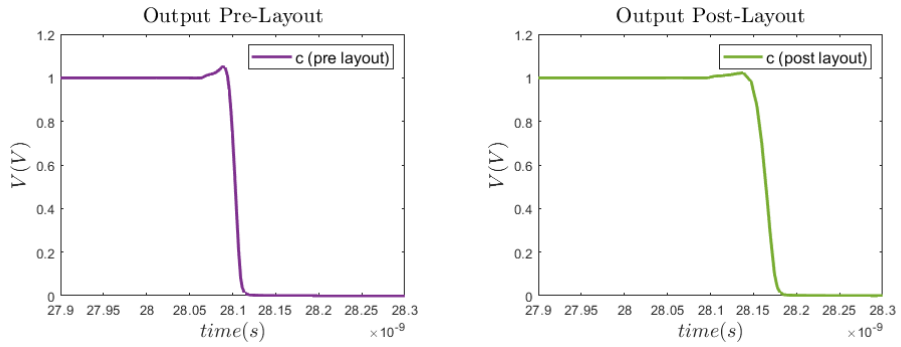


Figure 28: Zoomed in View of Pre and Post-Layout Output Transitioning from High to Low

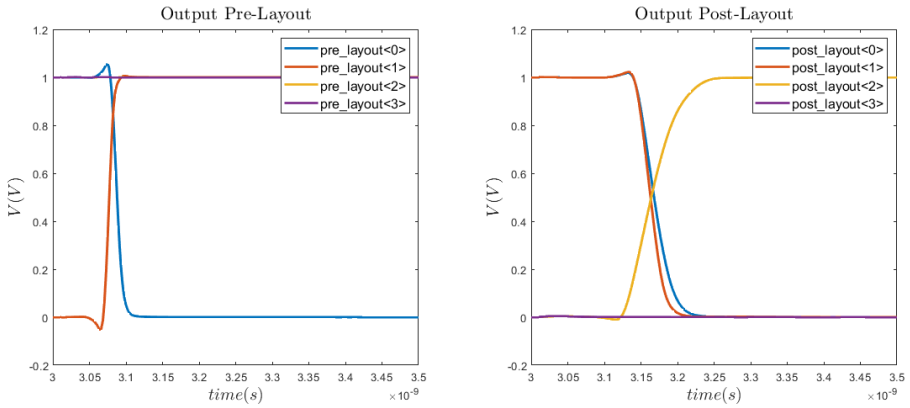


Figure 29: Zoomed in View of Pre and Post-Layout Output of 4-bit Verilog Counter

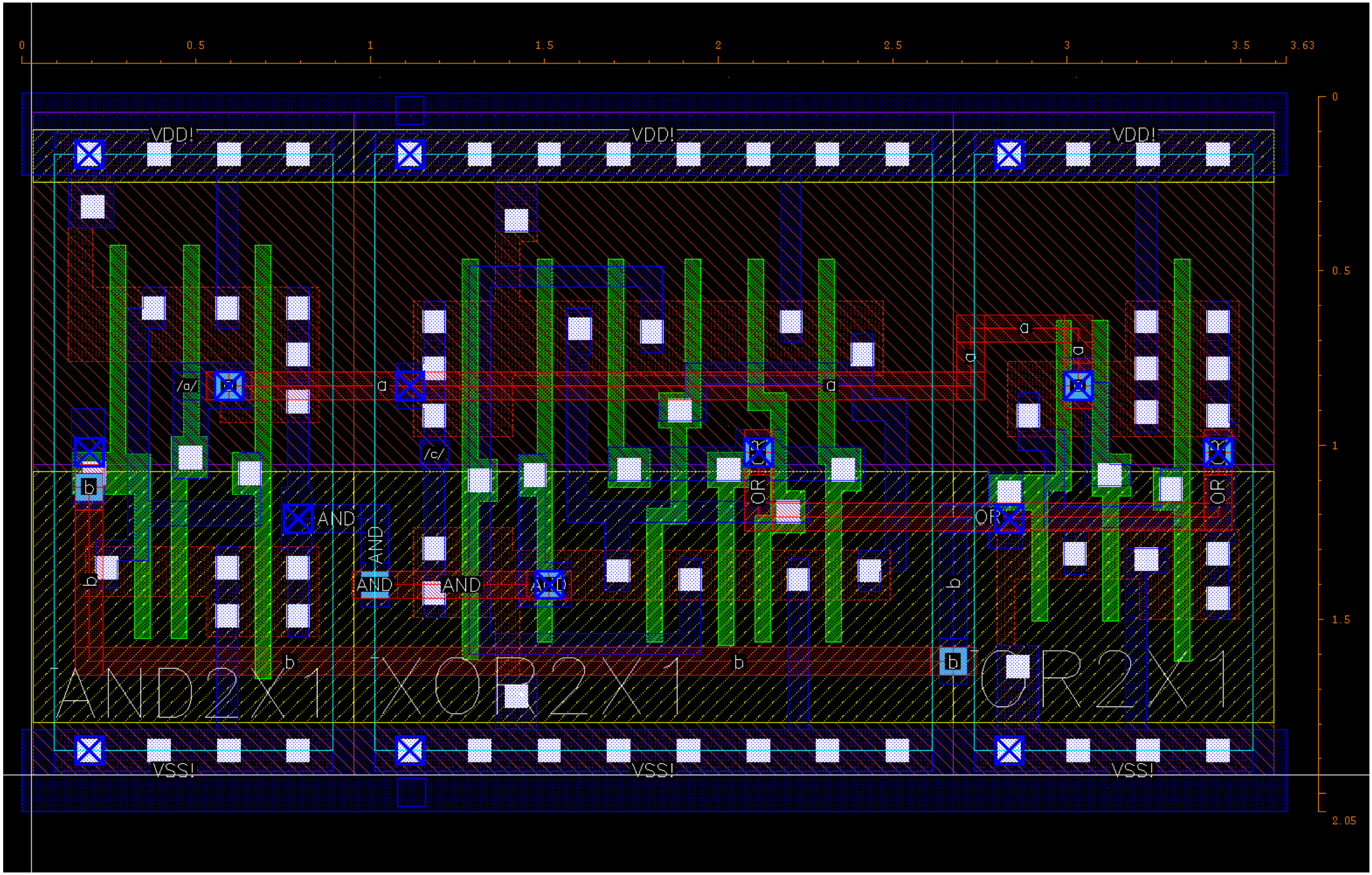


Figure 30: Manual Layout of Three Gate Logic Function

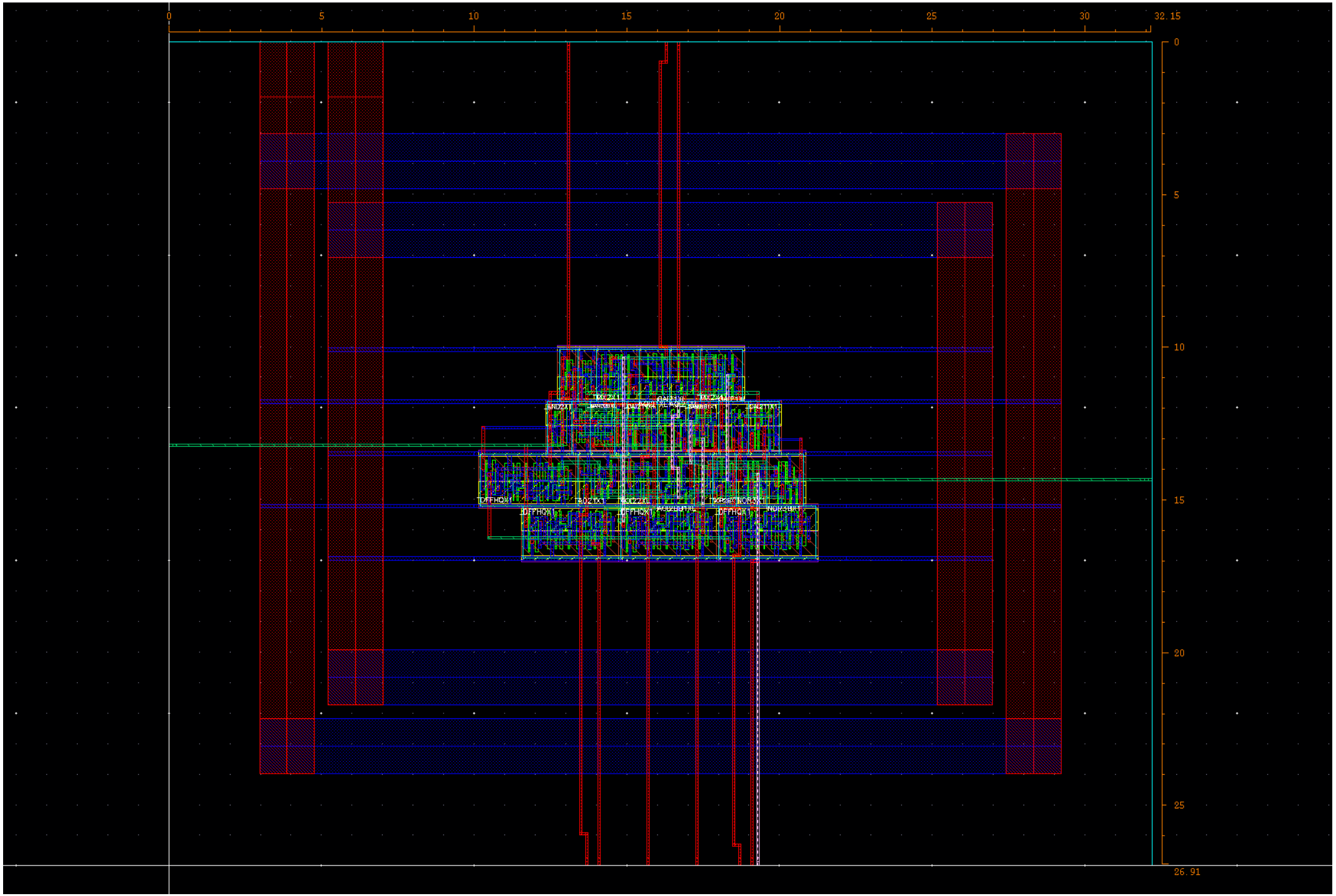


Figure 31: Automatic Layout of `counter.v` Verilog File

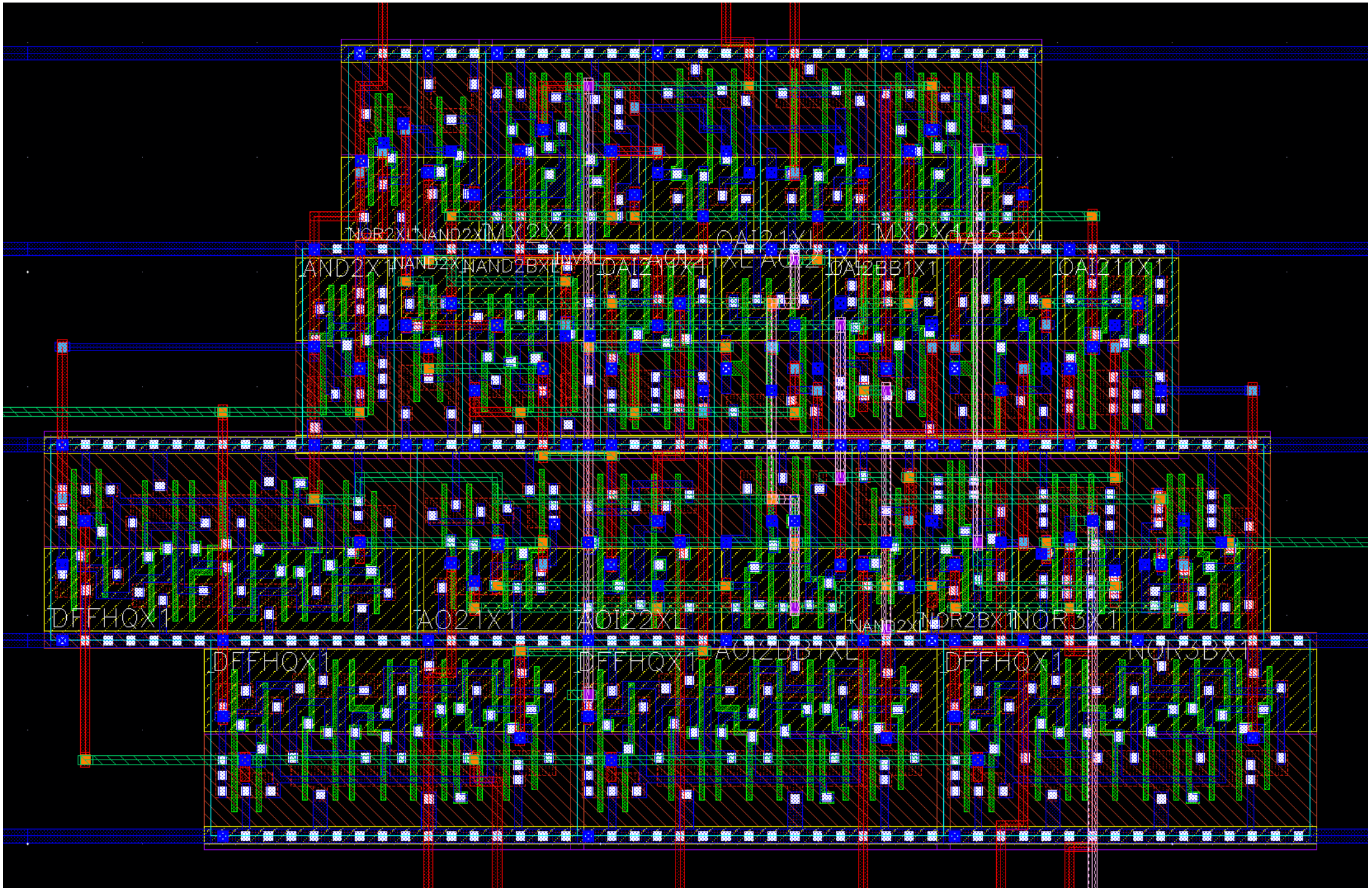


Figure 32: Zoomed in Automatic Layout of `counter.v` Verilog File

B Supplementary Tables

T_{period}	T_{int}	f	$V_{out-peak}$	I_{in}	Transimpedance Gain
$100\mu s$	$50\mu s$	$10kHz$	$3.3V$ (sat)	$1\mu A$	-
$80\mu s$	$40\mu s$	$12.5kHz$	$3.3V$ (sat)	$1\mu A$	-
$60\mu s$	$30\mu s$	$16.6kHz$	$2.94V$	$1\mu A$	2.94×10^6
$40\mu s$	$20\mu s$	$25kHz$	$1.95V$	$1\mu A$	1.95×10^6
$20\mu s$	$10\mu s$	$50kHz$	$0.975V$	$1\mu A$	0.975×10^6
$10\mu s$	$5\mu s$	$100kHz$	$0.484V$	$1\mu A$	0.484×10^6

Table 1: Relationship Between Frequency (f) and Gain for Charge Amplifer, $C_{int} = 10pF$

$$c = ((a\ AND\ b)\ XOR\ (a\ OR\ b)) \tag{4}$$

a	**b**	**c**
0	0	0
0	1	1
1	0	1
1	1	0

Table 2: Logic Table for Logic Circuit Manually Implemented in Lab 3